Faculty of Engineering

DEPARTMENT of ELECTRICAL AND ELECTRONIC ENGINEERING

EENG (INFE)115 Introduction to Logic Design

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Final EXAMINATION

January 14, 2016

Duration: 120 minutes

Number of Questions: 4

Good Luck

STUDENT'S	
NUMBER	
NAME	SOLUTIONS
SURNAME	

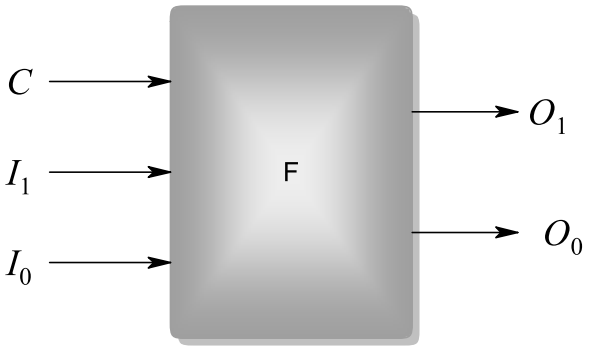
Question		Points
1		30
2		30
3		30
4		30
TOTAL		120

Read the following instructions carefully:

1. **Calculators** are not allowed.
2. Switch off **mobile phones** and **do not borrow** any stationery from your friends.
3. In your solutions, **show all details** you claim credit for.

Question 1

A combinational circuit has three inputs (C, I_1, I_0) and two outputs (O_1, O_0) :



The function implemented by F is the following: If $C = 0$, then O_1O_0 becomes I_1I_0 . If $C = 1$, then O_1O_0 becomes (I_1I_0)+1. For example, if $C = 1$and I_1I_0 is 01, O_1O_0 becomes 10. Note that if I_1I_0 is 11 and $C = 1$, then the output value wraps around 00, without any overflow.

a) Fill the Truth Table.

C	I_1	I_0	O_1	O_0
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	0

b) Write the Boolean expression for O_1 and O_0 in sum of minterms form.

$$O_1 = \sum(2,3,5,6)$$
$$O_0 = \sum(1,3,4,6)$$

c) Fill in the K-Maps for O_1 and O_0, and find the Boolean expression for the minimum sum of products implementation.

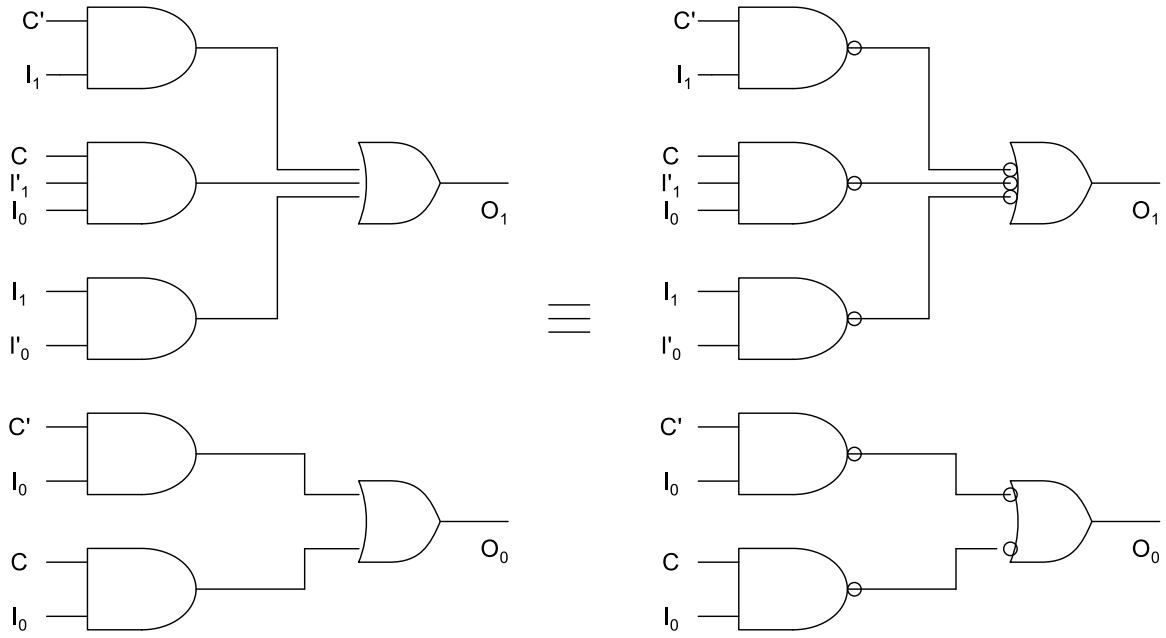
C \ I_1I_0	00	01	11	10
0			1	1
1		1		1

$$O_1 = C'I_1 + I_1I_0' + CI_1'I_0 = I_1 \oplus (CI_0)$$

C \ I_1I_0	00	01	11	10
0		1	1	
1	1			1

$$O_0 = C'I_0 + CI_0' = C \oplus I_0$$

d) Draw the logic diagram for O_1 and O_0. Then convert all gates with NAND gates.



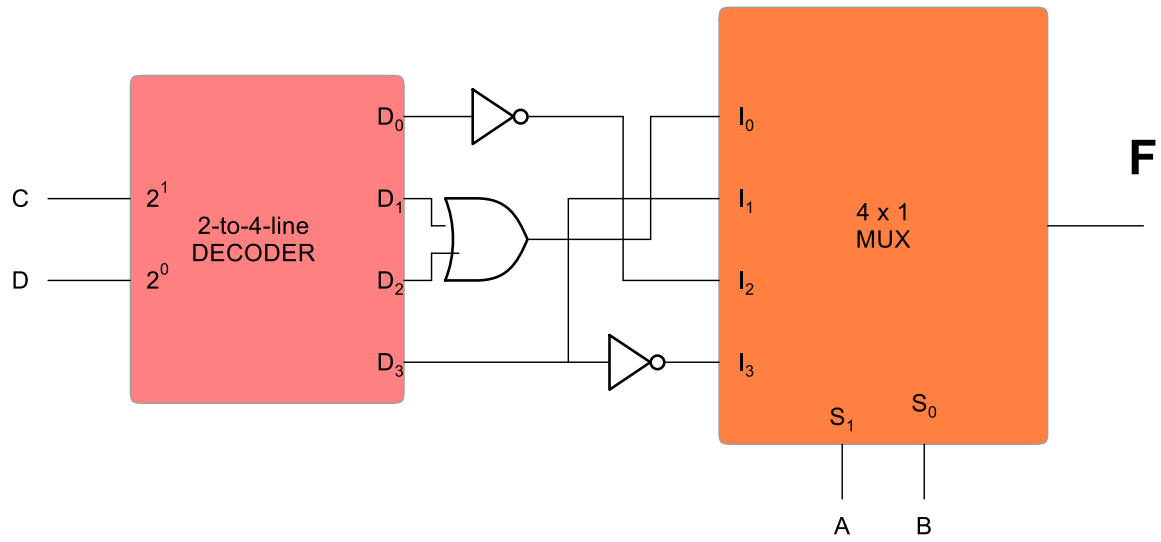
Question 2

Implement the following Boolean function with a 4×1 multiplexer, a 2-to-4-line decoder, two inverters and an OR gate.

$$F(A,B,C,D) = ABC'+AB'C+ABD'+AB'D+A'B'CD'+A'BCD+A'B'C'D$$

Connect inputs A and B to the selection lines of the multiplexer.

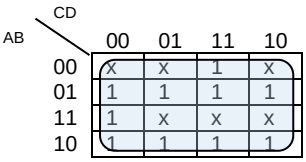
A	B	C	D	F	
0	0	0	0	**0**	**I_0=C'D+CD'**
0	0	0	1	**1**	
0	0	1	0	**1**	
0	0	1	1	**0**	
0	1	0	0	**0**	**I_1=CD**
=0	1	0	1	**0**	
0	1	1	0	**0**	
0	1	1	1	**1**	
1	0	0	0	**0**	**I_2=C+D=(C'D')'**
1	0	0	1	**1**	
1	0	1	0	**1**	
1	0	1	1	**1**	
1	1	0	0	**1**	**I_3=C'+D'=(CD)'**
1	1	0	1	**1**	
1	1	1	0	**1**	
1	1	1	1	**0**	



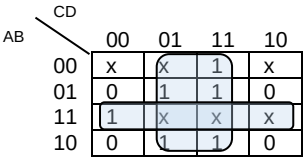
Question 3

Use T flip-flops to design a synchronous decimal counter that counts the repeated Excess-3 binary sequence; 0011 to 1100. Treat unused states as don't care conditions.

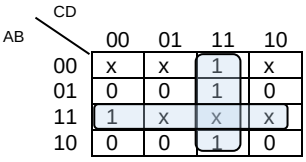
Present State				Next State				Flip-Flop Inputs			
A	B	C	D	A	B	C	D	T_A	T_B	T_C	T_D
0	0	0	0					X	X	X	X
0	0	0	1					X	X	X	X
0	0	1	0					X	X	X	X
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	0	0	1	1	1	1	1	1
1	1	0	1					X	X	X	X
1	1	1	0					X	X	X	X
1	1	1	1					X	X	X	X



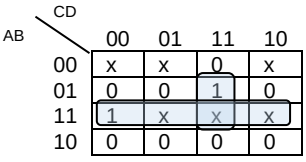
$$T_D = 1$$



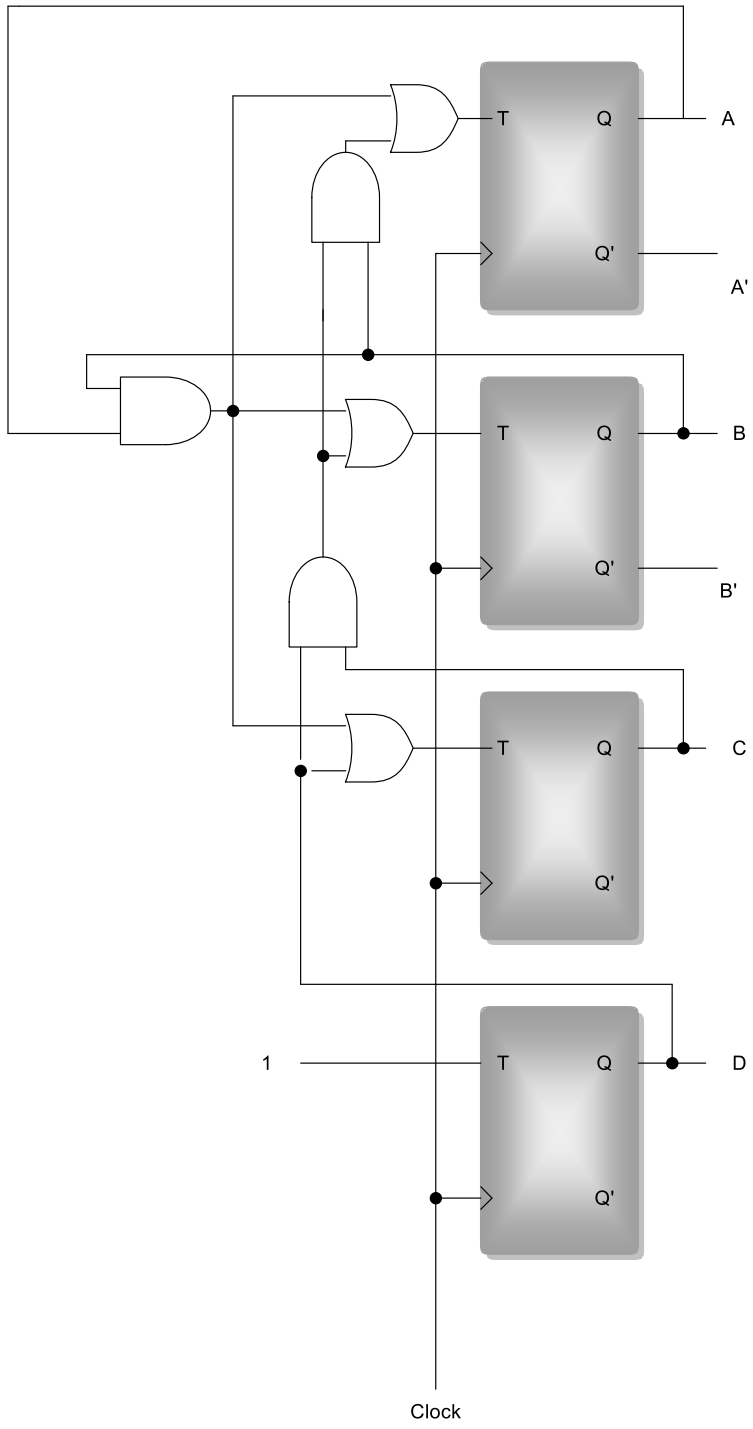
$$T_C = AB + D$$



$$T_B = CD + AB$$



$$T_A = AB + BCD$$


T
Q
A
Q'
A'
T
Q
B
Q'
B'
T
Q
C
Q'
1
T
Q
D
Q'
Clock

Question 4

Consider the synchronous sequential circuit whose state table is given below. The circuit has one input x and one output y. Design the circuit using

a) **D flip-flops**.
b) **T flip-flops**
c) Which design is simpler; i.e.; uses less number of gates, (a) or (b)?

Present State		Input	Next State		Output	Flip-Flop Inputs			
A	B	x	A	B	y	D_A	D_B	T_A	T_B
0	0	0	1	0	1	1	0	1	0
0	0	1	0	1	0	0	1	0	1
0	1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1	0
1	0	1	0	0	1	0	0	1	0
1	1	0	0	1	0	0	1	1	0
1	1	1	0	1	1	0	1	1	0

A \ Bx	00	01	11	10
0	1	0	0	1
1	0	0	0	0

$D_A = A'x'$

A \ Bx	00	01	11	10
0	0	1	0	1
1	0	0	1	1

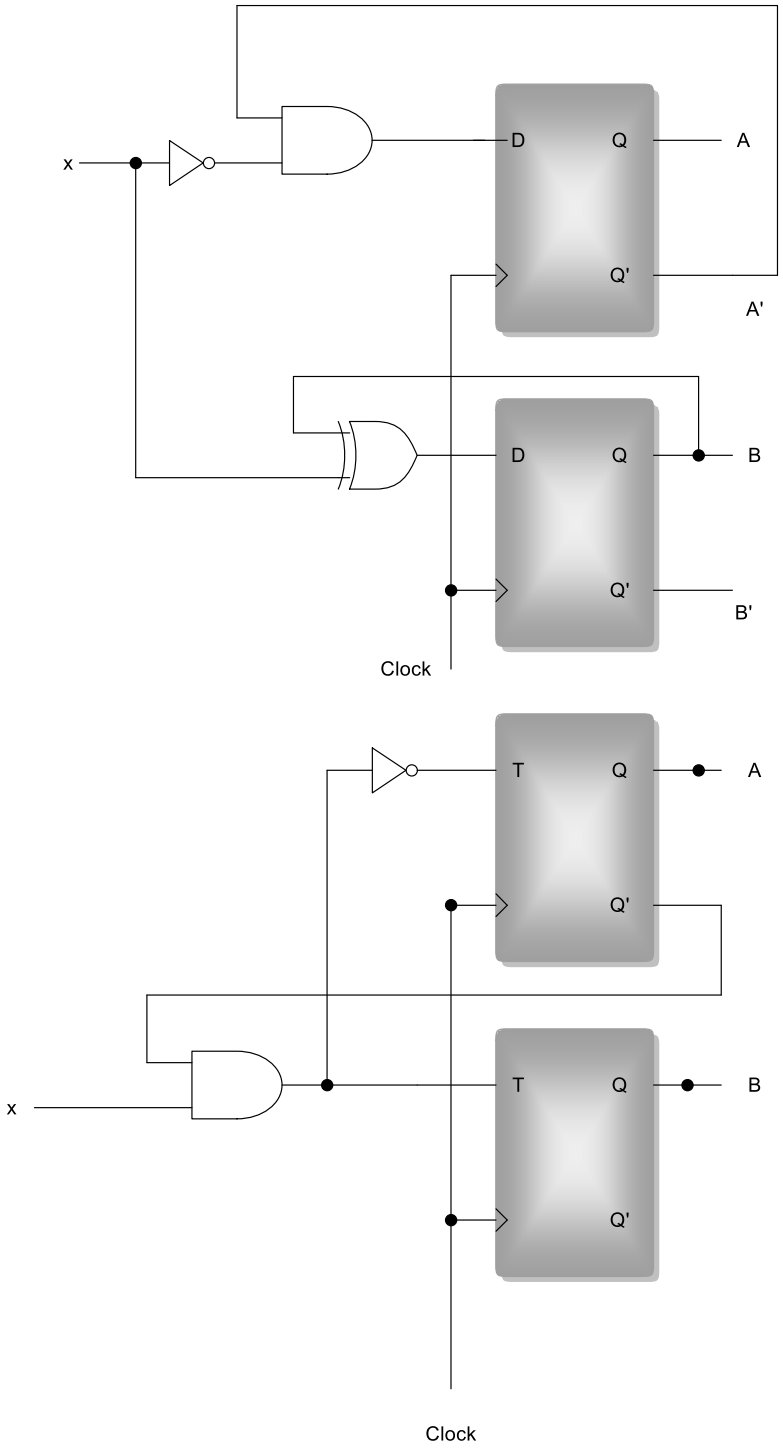
$D_B = A'B'x+AB+Bx'=B \oplus (A'x)$

A \ Bx	00	01	11	10
0	1	0	0	1
1	1	1	1	1

$T_A = A+x'$

A \ Bx	00	01	11	10
0	0	1	1	0
1	0	0	0	0

$T_B = A'x$



T design is simpler than D design.