HOMEWORK II - ANSWERS

DUE: Group1, <u>Wednesday 24 MAY 2017</u> and Group2, <u>Thursday 25 MAY 2017</u> <u>Tuesday!</u>

1. Design a combinational code converter that converts a **4-bit** gray code to binary number. **(20 pts.)**

	Gray Code				Binary			
Decimal	A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	1	1	0	1	1	0	0	1
10	1	1	1	1	1	0	1	0
11	1	1	1	0	1	0	1	1
12	1	0	1	0	1	1	0	0
13	1	0	1	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	0	1	1	1	1

w's K-MAP

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

x = A

x's K - MAP

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	1	0
10	1	1	1	1

x = A'B + AB' = $A \oplus B$

y's K-MAP

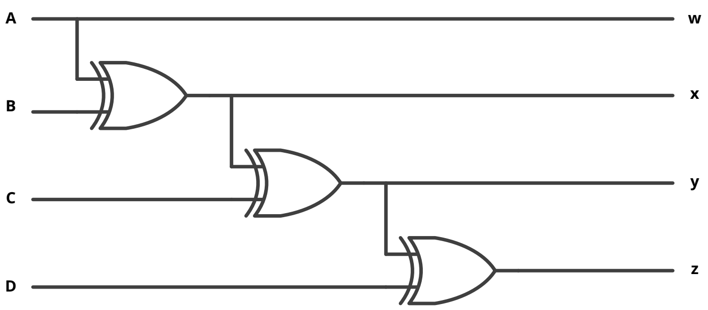
AB \ CD	00	01	11	10
00	**0**	**0**	**1**	**1**
01	**1**	**1**	**0**	**0**
11	**0**	**0**	**1**	**1**
10	**1**	**1**	**0**	**0**

$y = A \oplus B \oplus C$

z's K - MAP

AB \ CD	00	01	11	10
00	**0**	**1**	**0**	**1**
01	**1**	**0**	**1**	**0**
11	**0**	**1**	**0**	**1**
10	**1**	**0**	**1**	**0**

$z = A \oplus B \oplus C \oplus D$



2. Design a combinational circuit with three inputs, *A*, *B*, and *C*, and three outputs, *x*, *y*, and *z* . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input. **(16 pts.)**

A	B	C	x	y	z
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1

x's K-MAP

A \ BC	00	01	11	10
0	0	0	1	0
1	0	0	1	1

x = BC + AB

y's K - MAP

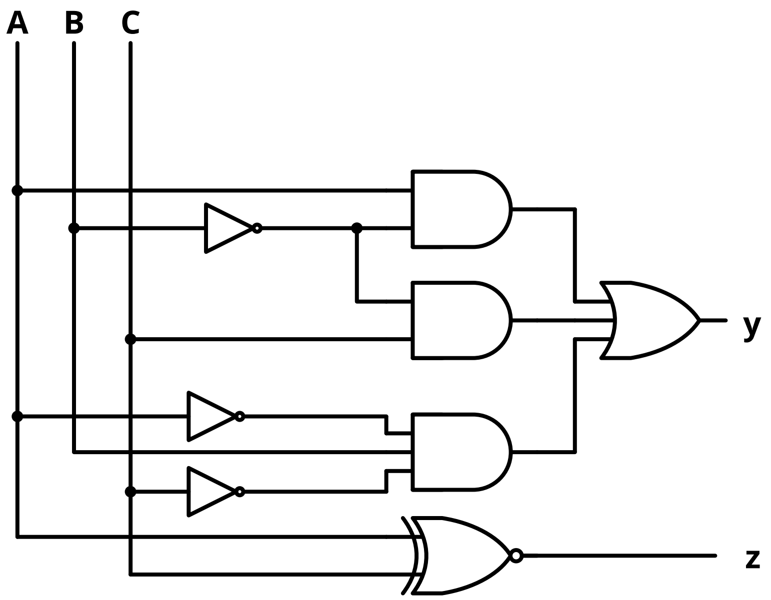
A \ BC	00	01	11	10
0	0	1	0	1
1	1	1	0	0

y = AB' + B'C + A'BC'

z's K-MAP

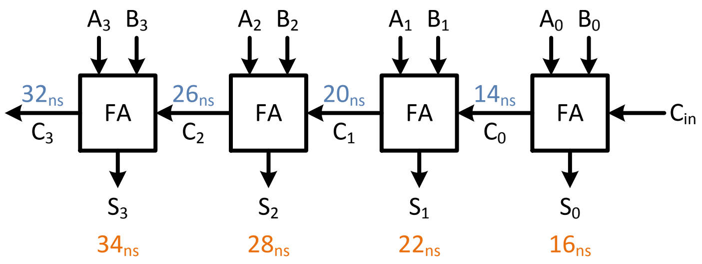
A \ BC	00	01	11	10
0	1	0	0	1
1	0	1	1	0

z = AC + A'C'



3. Assume that the exclusive-OR gate has a propagation delay of 8 ns and that the AND or OR gates have a propagation delay of 3 ns. What is the total propagation delay time in the four-bit adder? **(4 pts.)**

- **From Ai/Bi to Ci+1: 3 gate – levels (XOR → AND → OR) = $(8 + 3 + 3)_{ns}$ = 14ns**
- **From Ai/Bi to Si: 2 gate – levels (XOR → XOR)= $(8 + 8)_{ns}$ = 16ns**
- **From Ci/Ci+1: 2 gate levels (AND → OR)= $(3+3)_{ns}$ = 6ns**
- **Total Propagation delay time for a 4-bit adder:**

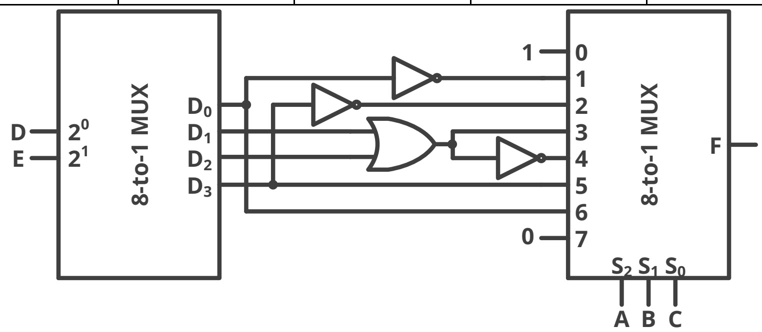


4. Implement the following Boolean function with a **8×1 multiplexer**, a **2-to-4-line decoder**, **3 x inverters** and a **OR-gate**. **(20 pts.)**

$$F(A, B, C, D, E) = \sum (0,1,2,3,5,6,7,8,9,10,13,14,16,19,23,24)$$

A	B	C	D	E	F	
0	0	0	0	0	1	1
0	0	0	0	1	1	
0	0	0	1	0	1	
0	0	0	1	1	1	
0	0	1	0	0	0	D + E = (D'.E')'
0	0	1	0	1	1	
0	0	1	1	0	1	
0	0	1	1	1	1	
0	1	0	0	0	1	(D.E)'
0	1	0	0	1	1	
0	1	0	1	0	1	
0	1	0	1	1	0	
0	1	1	0	0	0	D'.E+D.E'
0	1	1	0	1	1	
0	1	1	1	0	1	
0	1	1	1	1	0	
1	0	0	0	0	1	(D'.E+D.E')'
1	0	0	0	1	0	

1	0	0	1	0	0	
1	0	0	1	1	1	
1	0	1	0	0	0	D.E
1	0	1	0	1	0	
1	0	1	1	0	0	
1	0	1	1	1	1	
1	1	0	0	0	1	D'E'
1	1	0	0	1	0	
1	1	0	1	0	0	
1	1	0	1	1	0	
1	1	1	0	0	0	0
1	1	1	0	1	0	
1	1	1	1	0	0	
1	1	1	1	1	0	



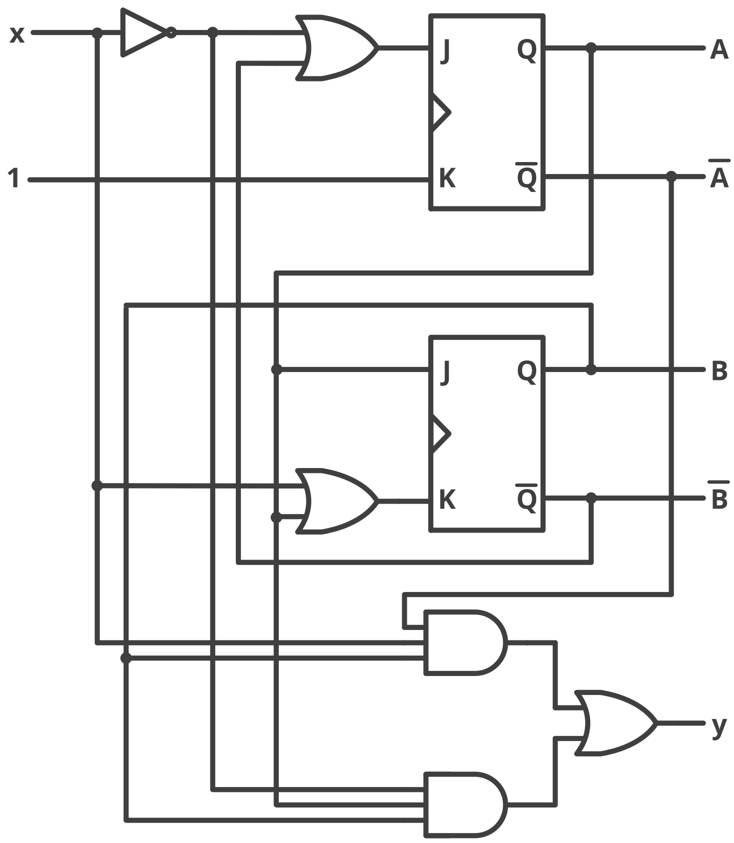
5. Sequential circuit that has two flip-flops A and B and one input x and a constant '1'. It consists of a combinatorial logic connected to the JK flip-flops, as shown in Figure below.

a) Derive the next state and output equations.

b) Derive the state table of the sequential circuit.

c) Draw the corresponding state diagram.

(20 pts.)



a)

- **JA = B′ + x′, JB = A**
- **KA =1, KB = A + x**
- **y = A′.B.x + A.B.x′**
- QA(t+1) = JA.A′ + KA′A = (B′+x′) A′ + (0) A

  = **A′B′ + A′x′**
- QB (t+1) = JB.B′ + KB′B = A.B′ + (A+x)′ B

  = **AB′ + A′Bx′**
- y = **A′Bx + ABx′**

b)

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	1	1	0

0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

c)