Faculty of Engineering

DEPARTMENT of ELECTRICAL AND ELECTRONIC ENGINEERING

EENG447

Digital IC Design

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Mini Project

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Good Luck

About

Arithmetic logic unit (ALU) shown in Figure 1 is a critical component of a microprocessor and is the mathematical core of a central processing unit (CPU). Typically, it is a combinational logic circuit that performs logical (AND, OR, XOR) and arithmetical operations (addition, subtraction, shift, complement, negate, and magnitude comparison).

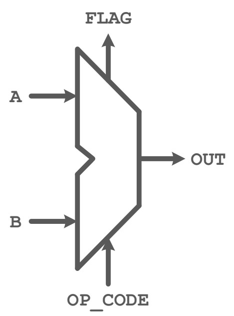


Figure 1: ALU Symbol

Architecture

The architecture of an 8-bit ALU core is shown Figure 2. ALU core consists of a three main units; Arithmetic, logic and shifter units. These units are controlled by a control unit and the output data is stored in a storage unit.

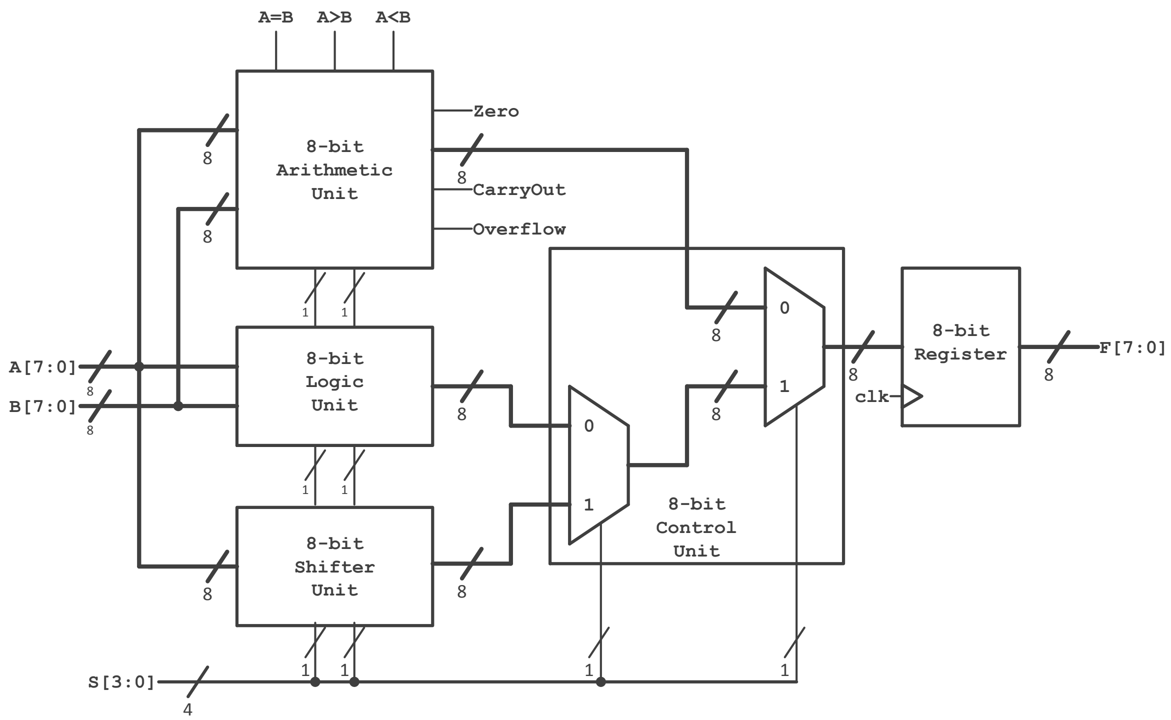


Figure 2: 8-bit ALU Architecture.

Functional Specifications

ALU is controlled by the four function inputs (S3 to S0). These inputs control 8-bit 2-to-1 multiplexers inside and outside of the logic blocks. Table 1 shows the operation codes that ALU performs based on the select inputs.

Table 1: Operation Codes.

S_0	S_1	S_2	S_3	F	Description
0	0	0	0	**A+B**	**Add**
0	0	0	1	**A-B**	**Subtract**
0	0	1	1	**B′+1**	**2′s Complement**
1	0	0	0	**A AND B**	**AND**
1	0	0	1	**A XOR B**	**XOR**
1	0	1	0	**A OR B**	**OR**
1	0	1	1	**B′**	**1′s Complement**
1	1	0	0	**A → →**	**RIGHT ROTATE**
1	1	0	1	**← ← A**	**LEFT ROTATE**
1	1	1	0	**A →**	**RIGHT SHIFT**
1	1	1	1	**← A**	**LEFT SHIFT**

Arithmetic Unit:

Arithmetic unit shown in Figure 4, performs addition, subtraction and negate (2’s complement) operation of two numbers (A and B) using an 8-bit ripple carry adder and an 8-bit negate block which consists of an 8-bit 2-to-1 multiplexer and an 8-bit ripple carry adder. Additionally, arithmetic unit also compare two numbers (A and B) using an 8-bit magnitude comparator. Each of these blocks is described in the following sections.

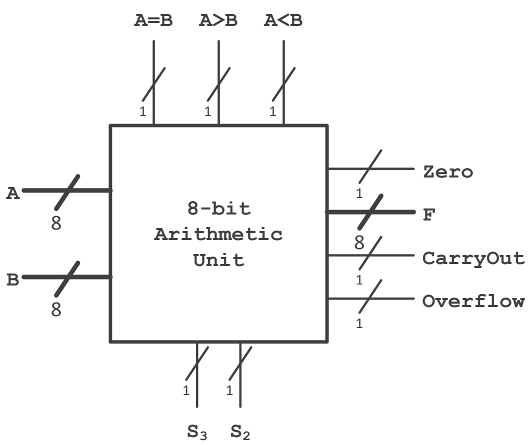


Figure 3: Arithmetic Unit Symbol.

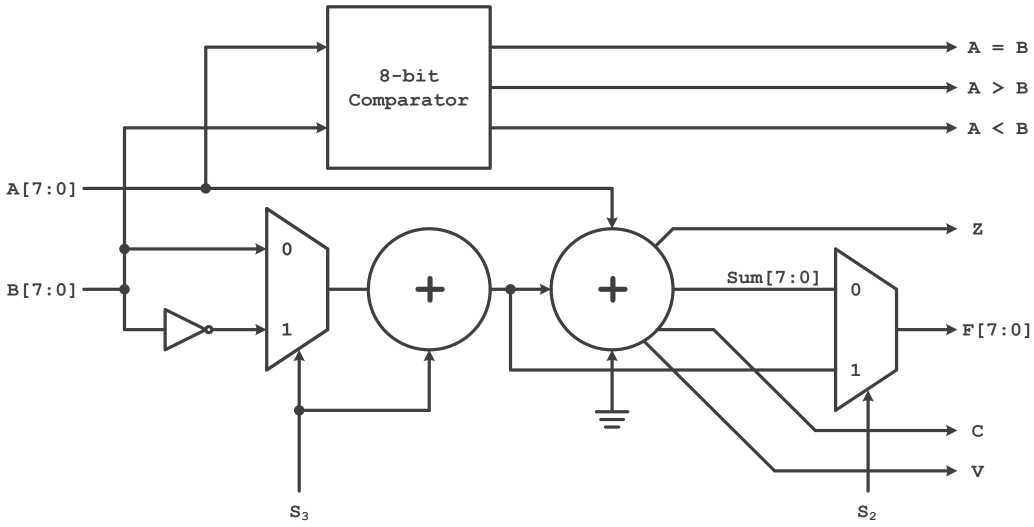


Figure 4: Arithmetic Unit Architecture.

2’s Complement

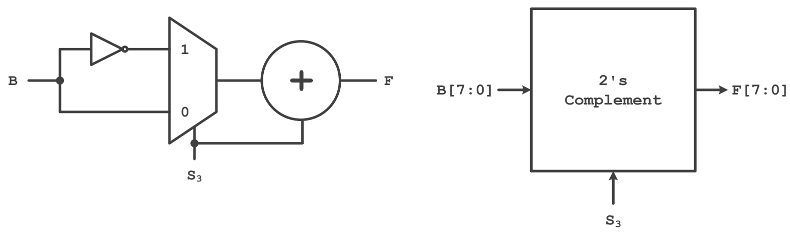
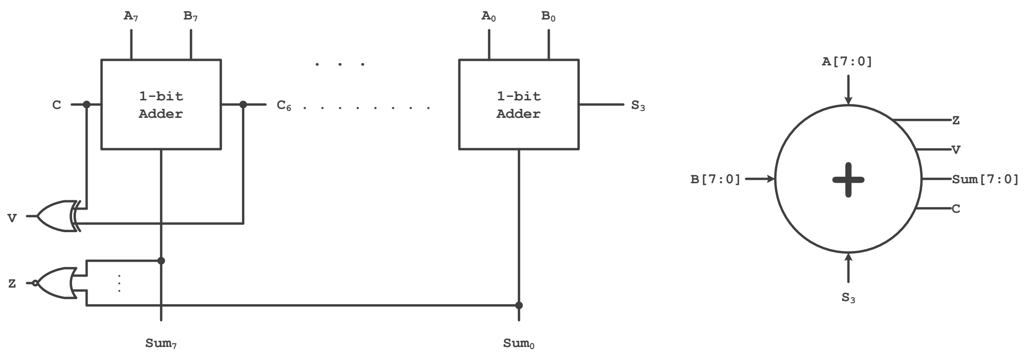


Figure 5: 2's Complement Logic Block and Symbol.

Table 2: 2's Complement Op Codes.

S_3	Function
0	B
1	B’+ 1

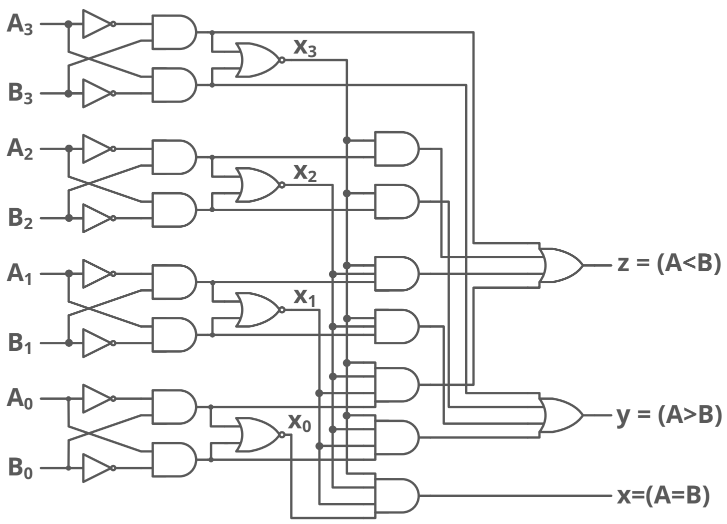
Adder Circuitry:



S_3	Function
0	A + B
1	A - B

Comparator Circuitry:

This is as an example of 4-bit implementation, this need to be extended to 8-bits.



$x_3 = A_3' . B_3' + A_3 . B_3$
$x_2 = A_2' . B_2' + A_2 . B_2$
$x_1 = A_1' . B_1' + A_1 . B_1$
$x_0 = A_0' . B_0' + A_0 . B_0$
$x = x_3 . x_2 . x_1 . x_0 = (A = B)$

$y_3 = A_3 . B_3'$
$y_2 = x3 . A_2 . B_2'$
$y_1 = x3 . x2 . A_1 . B_1'$
$y_0 = x3 . x2 . x1 . A_0 . B_0'$
$y = y_3 + y_2 + y_1 + y_0 = (A > B)$

$z_3 = A_3' . B_3$
$z_2 = x3 . A_2' . B_2$
$z_1 = x3 . x2 . A_1' . B_1$
$z_0 = x3 . x2 . x1 . A_0' . B_0$
$z = z_3 + z_2 + z_1 + z_0 = (A < B)$

Logic Unit:

Logic Unit shown in Figure 6 performs bit wise AND, OR, XOR and Invert operations. Multiplexers used to select different operations.

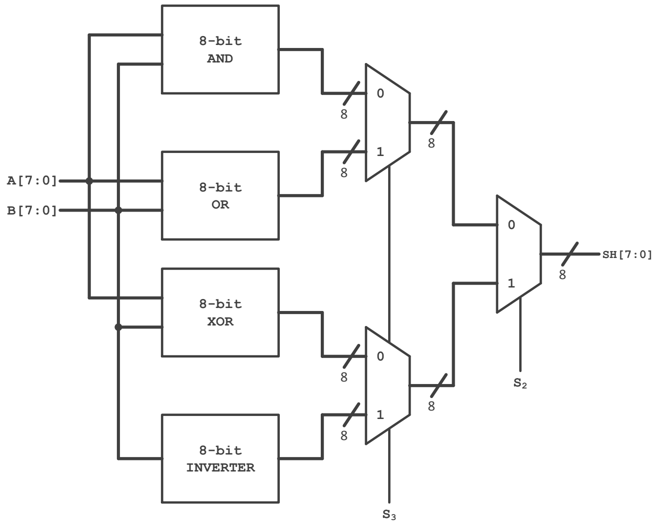


Figure 6: Logic Unit Architecture.

S_3	S_2	Function
0	0	A AND B
0	1	A XOR B
1	0	A OR B
1	1	B’

Shifter Unit:

Shifter unit shown in Figure 7 performs right and left shift and rotate operations using 8-bit 2-to1 multiplexers. Shifter operations are explained in details in Figure 8

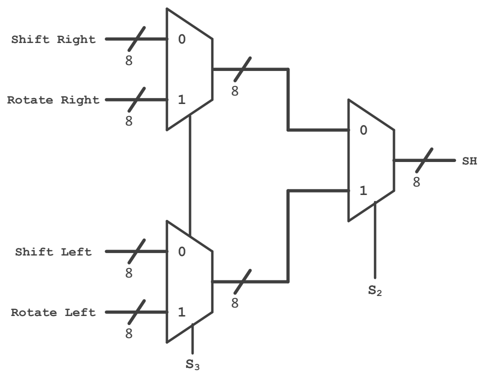


Figure 7: Shifter Unit Architecture.

S_3	S_2	Function
0	0	Right shift
0	1	Left shift
1	0	Right rotate
1	1	Left rotate

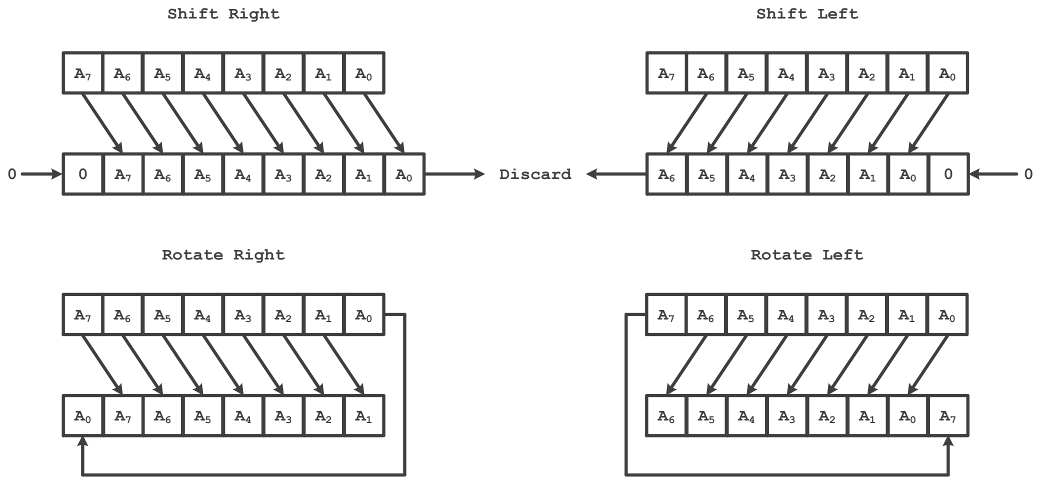


Figure 8: Shifter Operations.

Assignment…

1. Using hierarchical approach, design an 8-bit Arithmetic Logic Unit (ALU) schematic which performs the operations mentioned above. Show each logic block separately.
2. Using random test patterns simulate each logic gate, each logic block (Adder, Comparator, etc.) and each logic unit using T-Spice to verify the functionality of all your circuits.
3. Using hierarchical approach, design an 8-bit ALU's physical layout. Show each logic block separately.
4. Using Layout versus Schematic (LVS) compare your schematic design with layout to verify the connections.
5. Write a report to present your designs and your results.