Faculty of Engineering

DEPARTMENT of ELECTRICAL AND ELECTRONIC ENGINEERING

EENG447

Digital IC Design

Gürkan Yeniçeioğlu

Fall 2017-2018

Final Examination

Duration:120 mins

Number of Questions: 4

January 10, 2018

Good Luck

Student's	
NUMBER	
NAME	**SOLUTIONS**
SURNAME	

Question	Achieved	Points
1		30
2		40
3		40
4		10
TOTAL		120

Read the following instructions carefully:

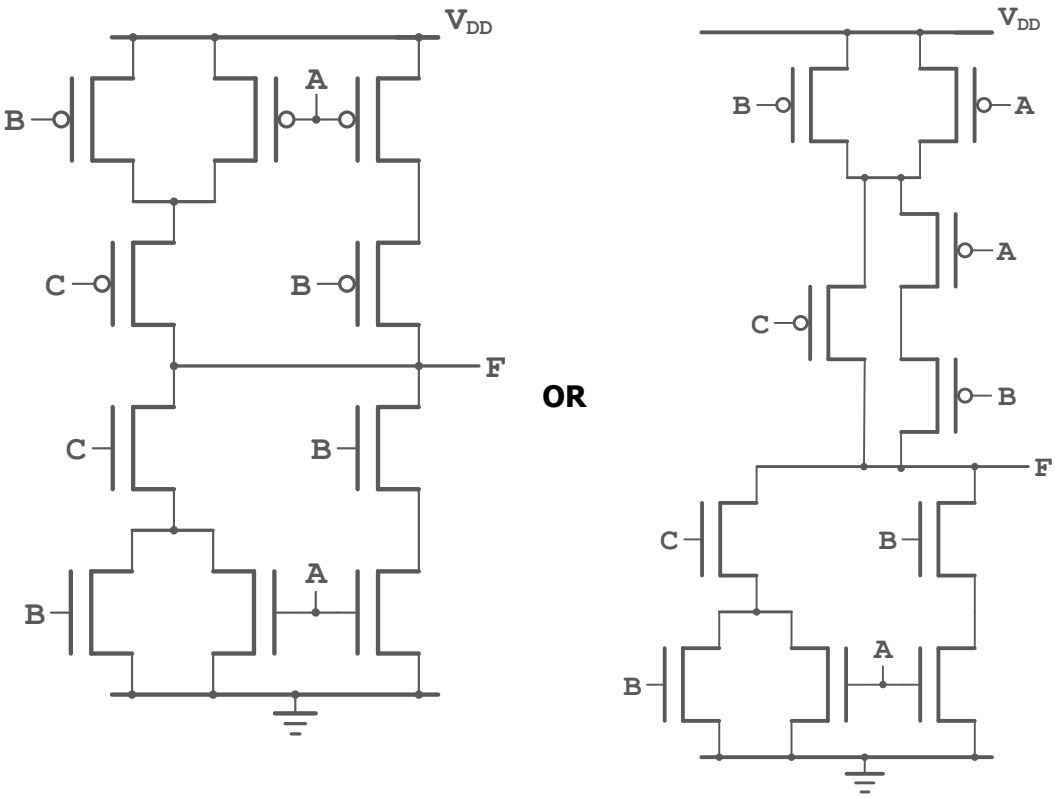
1. Switch off mobile phones and do not borrow any stationery from your friends.

2. In your solutions, show all details you claim credit for.

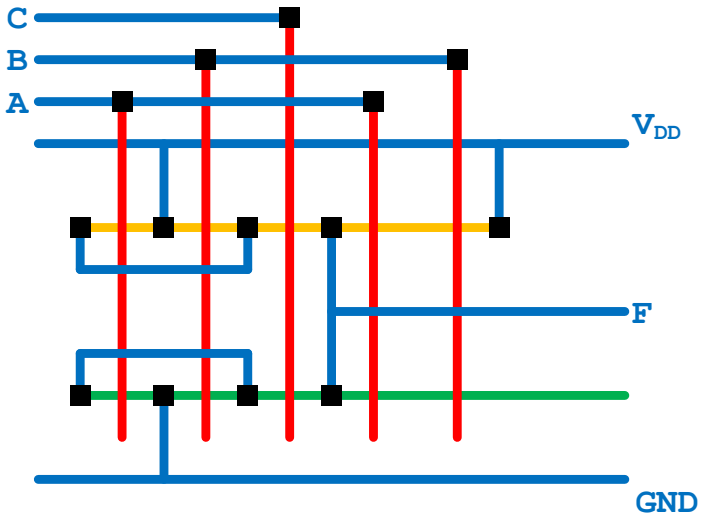
Question 1(30 pts):

Consider the logical expression **F = (AB + C (A+B))'.**

(a) Implement the given function to **transistor-level schematic** diagram for static CMOS logic. **Label** all the input, outputs and global ports. **(15 pts)**

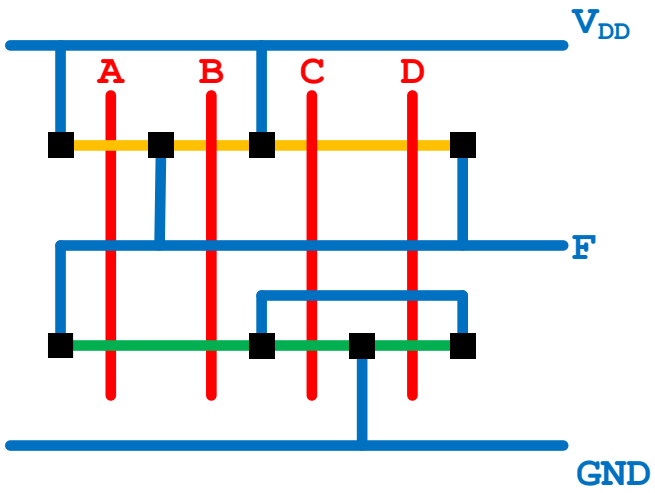


(b) Implement the given function to **stick diagram** layout. Make sure that the implemented circuit is **area efficient**. **Label** all the input, outputs and global ports.**(15 pts)**

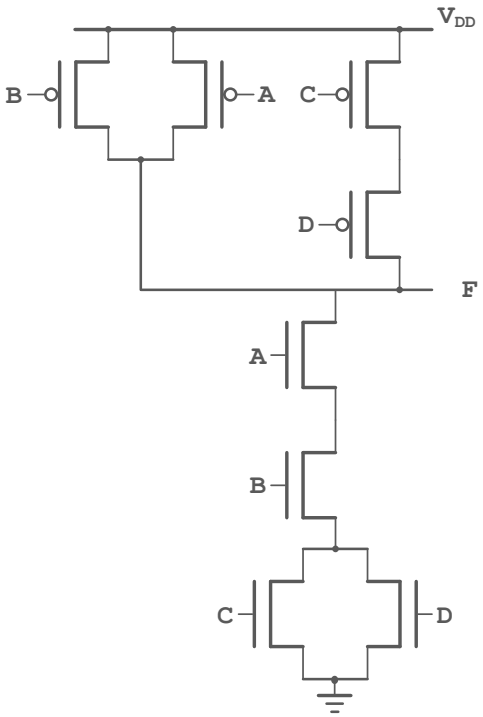


Question 2 (40 pts):

Consider the following stick diagram.

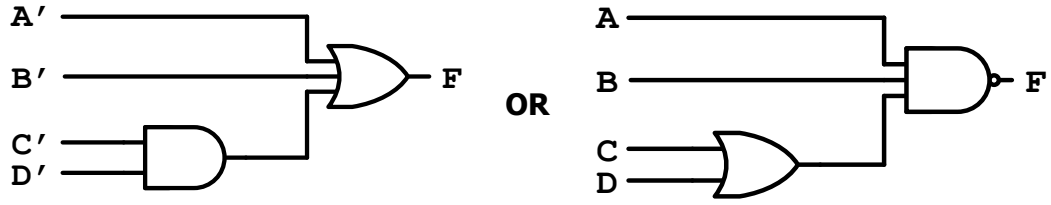


(a) Implement the electrically equivalent **transistor-level** schematic. **Label** all the input, outputs and global ports. **(15 pts)**



(b) What logic equation does the circuit implement? (**5 pts**)
F = A′ + B′ + C′ D′
F = (A B (C + D))′

(c) Implement the electrically equivalent **gate-level** logic circuit. (**5 pts**)

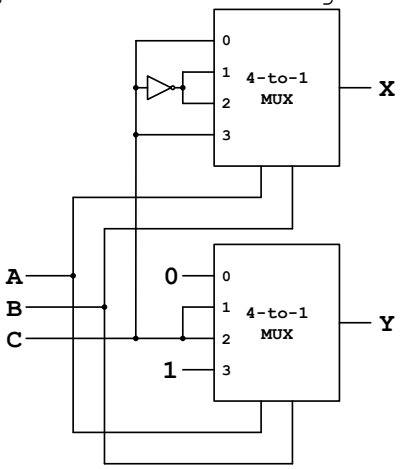


(d) For the **gate-level** logic circuit implemented in (c) design a set of tests to detect all **single-stuck faults**, showing all the faults covered by each test. **(15 pts)**

A	B	C	D	STACK FAULTS
0	0	0	0	F/0
0	0	0	1	F/0
0	0	1	0	F/0
0	0	1	1	F/0
0	1	0	0	F/0
0	1	0	1	A/1, F/0
0	1	1	0	A/1, F/0
0	1	1	1	A/1, F/0
1	0	0	0	C/1, F/0
1	0	0	1	B/0, F/0
1	0	1	0	B/0, F/0
1	0	1	1	B/0, F/0
1	1	0	0	C/1, D/1, X/1, F/0
1	1	0	1	A/0, B/0, D/0, X/0, F/1
1	1	1	0	A/0, B/0, C/0, X/0, F/1
1	1	1	1	A/0, B/0, C/0, X/0, F/1

Question 3(40 pts):

Consider the following combinational logic.



(a) Determine the functions ***X*** and ***Y*** as sums of minterms. You may use any process to determine the result, but show your work. **(10 pts)**

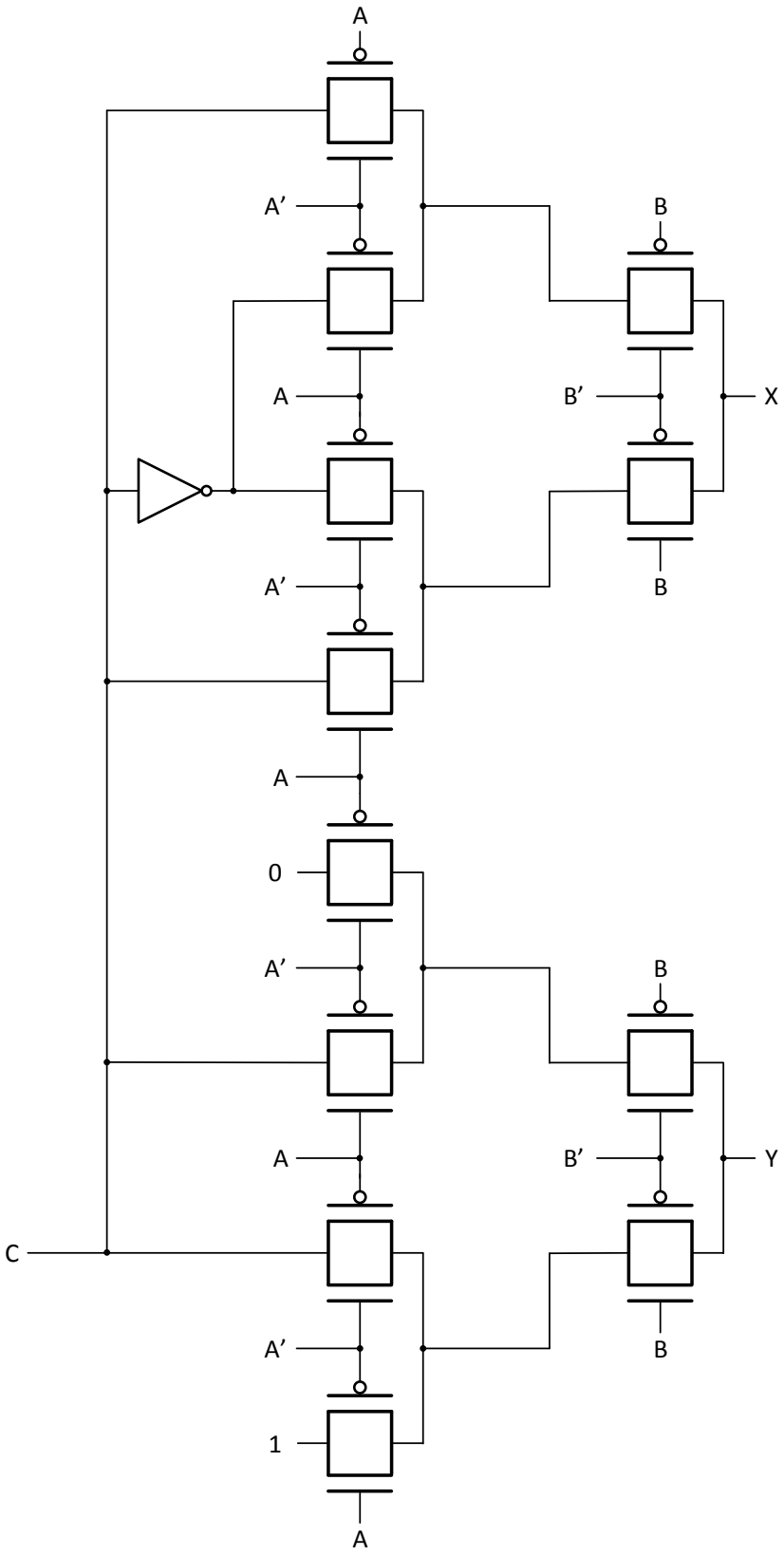
A	B	C	X	Y
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

X = ∑ (1, 2, 4, 7)
Y = ∑ (3, 5, 6, 7)

(b) What does the circuit do and what are other names for X and Y? **(2.5 pts)**

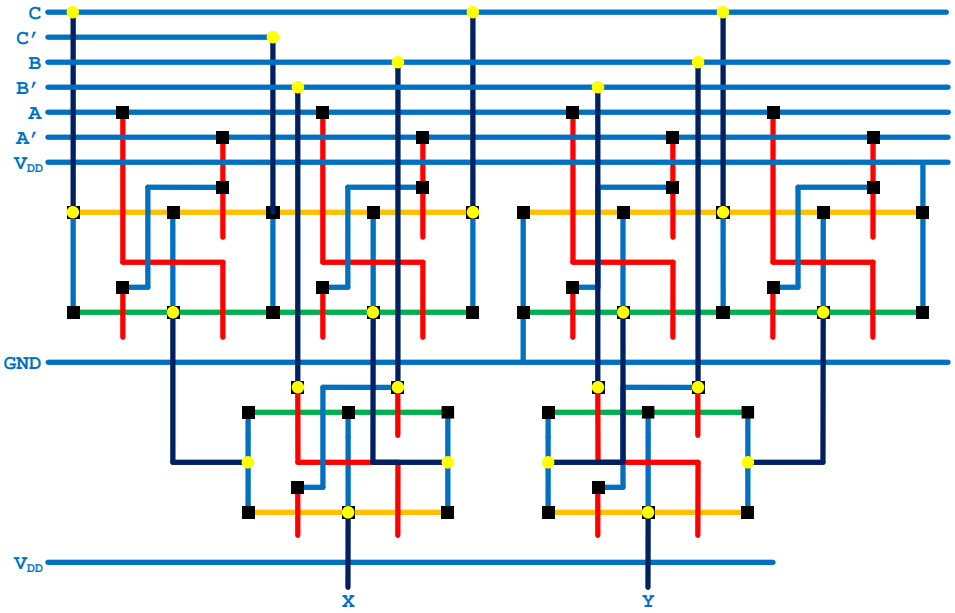
The circuit implements a FULL ADDER
X is the SUM
Y is the CARRY

(c) Implement the electrically equivalent **transistor-level** schematic for the circuit given. **Label** all the input, outputs and global ports. **(7.5 pts)**

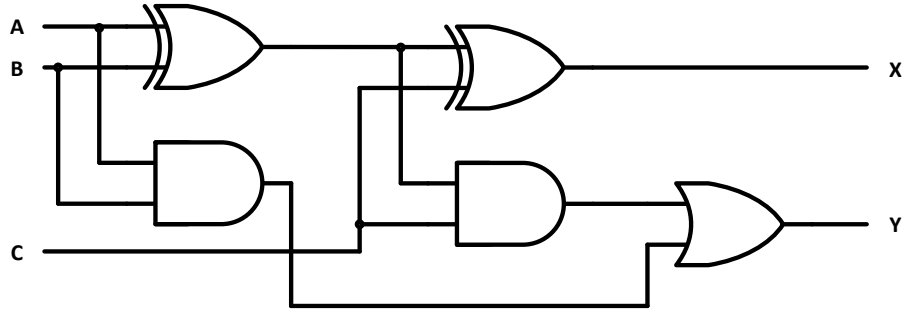


30 Transistors in total.

(d) Implement the given function to **stick diagram** layout. Make sure that the implemented circuit is **area efficient**. **Label** all the input, outputs and global ports. **(10 pts)**



(e) How many transistors are needed to implement the same circuit **without using multiplexers**? Use **gate-level implementation** and explain how this could be done? **(10 pts)**



ordinary XOR gate	**6 x PMOS + 6 x NMOS**	**12 transistors**
AND gate	**3 x PMOS + 3 x NMOS**	**6 transistors**
OR gate	**3 x PMOS + 3 x NMOS**	**6 transistors**
Full Adder	**2 x XOR + 2 AND + 1x OR** **2 x 12 + 2 x 6 + 1 x 6**	**42 transistors**
XOR gate with TG	**4 x PMOS + 4 x NMOS**	**8 transistors**
AND gate	**3 x PMOS + 3 x NMOS**	**6 transistors**
OR gate	**3 x PMOS + 3 x NMOS**	**6 transistors**
Full Adder	**2 x XOR + 2 AND + 1x OR** **2 x 6 + 2 x 6 + 1 x 6**	**34 transistors**

Question 4(10 pts):

Please explain the reason, why we usually implement the **Pull-up network** with **PMOS** and **Pull-Down network** with **NMOS.**

(Hint: You can show it by drawing the figure of the CMOS inverter.)

(10 pts)

Answer:

PMOS transistors can pass a strong "**1**" but a weak "**0**", and
NMOS transistors can pass a strong "**0**" but a weak "**1**".