EENG447 Lab Assessment I

Student No:	
Name and Surname:	

Due Date: 25.10.18

Weight: 5%

Task 1: Create CMOS_GATES library.

In CMOS_GATES library there will be CMOS transistor implementation of common gates shown in table 1.

Table 1: CMOS Gates Library

Gate Name	Description	Assessment
CMOS_INVERTER	– Inverter circuit.	
CMOS_BUFFER	– Buffer circuit.	
CMOS_AND	– AND gate circuit.	
CMOS_OR	– OR gate circuit.	
CMOS_NAND	– NAND gate circuit.	
CMOS_NOR	– NOR gate circuit.	
CMOS_MUX	– Multiplexer circuit.	
CMOS_TG	– Transmission gate circuit.	
CMOS_XOR	– XOR gate circuit.	
CMOS_XNOR	– XNOR gate circuit.	

Task 2: To test the functionality of the following circuits created in CMOS_GATES design;

1. Create another design "CMOS_GATES_TEST".
2. In this design you need to add CMOS_GATES library to your design.
3. For each CMOS gate create a separate test cell. For example: CMOS_AND_TEST.
4. Instantiate your CMOS_AND gate.
5. Instantiate input BIT/PULSE patterns
6. Instantiate supply voltage.
7. Simulate your design.
8. Save your timing waveform. For example: CMOS_AND_WAVE.
9. Repeat the steps 3 to 8 to have the table2 shown below.

Table 2: CMOS Gates Test Benches

Gate Name	Description	Assessment
CMOS_INVERTER_TEST	– Inverter circuit test bench.	
CMOS_BUFFER_TEST	– Buffer circuit test bench.	
CMOS_AND_TEST	– AND gate circuit test bench.	
CMOS_OR_TEST	– OR gate circuit test bench.	
CMOS_NAND_TEST	– NAND gate circuit test bench.	
CMOS_NOR_TEST	– NOR gate circuit test bench.	
CMOS_MUX_TEST	– Multiplexer circuit test bench.	
CMOS_TG_TEST	– Transmission gate circuit test bench.	
CMOS_XOR_TEST	– XOR gate circuit test bench.	
CMOS_XNOR_TEST	– XNOR gate circuit test bench.	

Note:

In your assessment;

Show your Schematic diagrams and simulation waveforms.

State what input patterns and supply voltage you have used.

To create schematics please refer to your lab manual.