Faculty of Engineering

Electrical and Electronics Engineering

EENG447

Digital IC Design

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Fall 2019

Midterm Exam

Duration: 90 min.

Number of Questions: 5

November 29, 2018

Good Luck

Student Number:	
Full Name:	

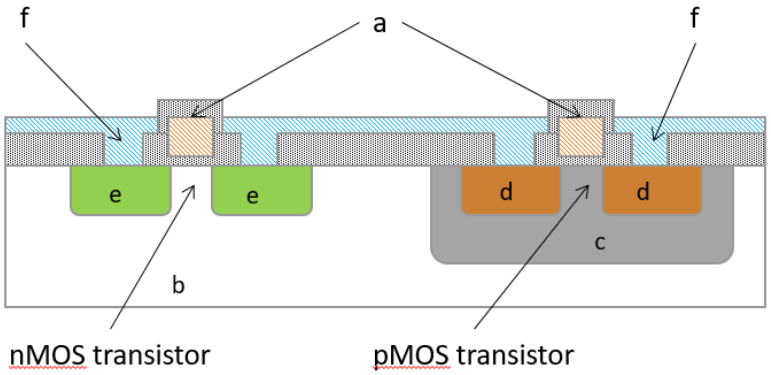
Question	Achieved	Points
1		10
2		28
3		18
4		24
5		20
TOTAL		100

1. This is a closed book examination. Calculators are *NOT ALLOWED*.
2. Please attempt all 5 questions, and clearly show the details of your work and reasoning for full credit.
3. Use the back side of the page if you need additional space to answer a question.

Question1 (10 pts.):

a. (5 pts) Define hierarchy and abstraction in the context of digital design. Briefly explain how hierarchy and abstraction are used to deal with design complexity.

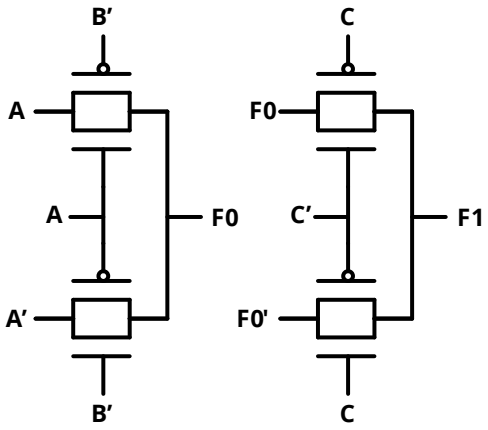
b. (5 pts) For the figure shown below label each of the letter with their corresponding masks. Order the letters based on the lithography process.



a = polysilicon
b = substrate
c = nwell
d = p+ diffusion
e = n+ diffusion
f = metal

Question2 (28 pts.): Sketch transistor-level schematics and truth table for the following:

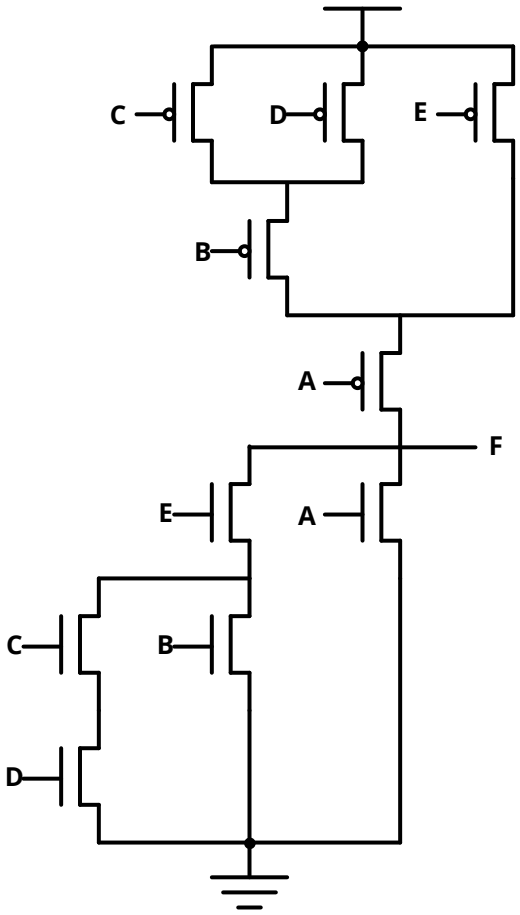
a. (4 pts) **3-input** CMOS **XNOR** gate.



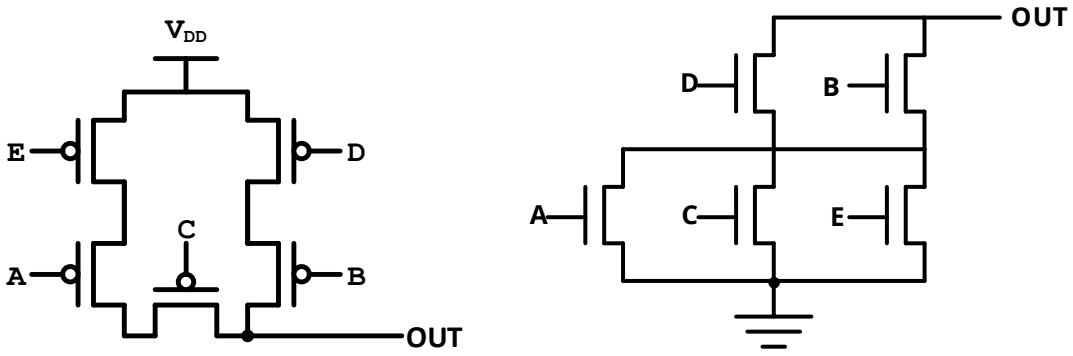
b. (8 pts) Complex gate function **F=[A+E(B+CD)]'.**

Assume the inputs are available in both the complemented and uncomplemented forms. Your design must consist of only a single stage of logic.

F' = A'(E'+(B'(C'+D')

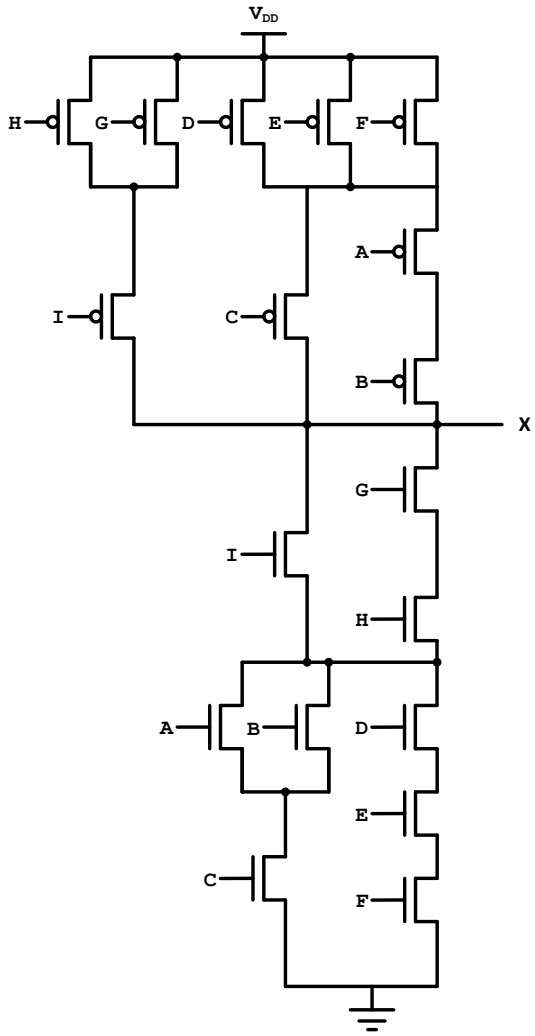


c. (4 pts) Design a pull-down circuit corresponding to the pull-up circuit shown below for implementing the function

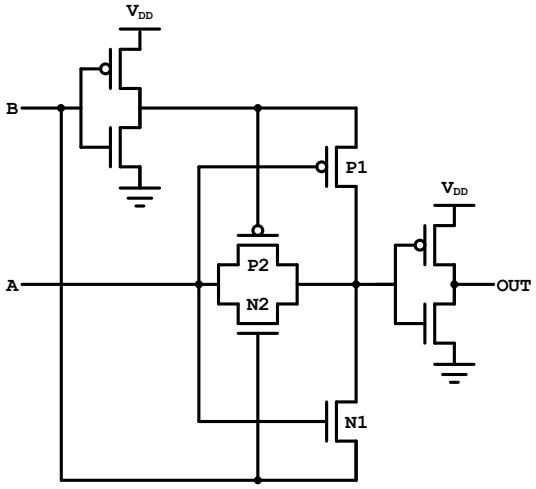


d. (4 pts) Analyse the CMOS logic circuit shown below and write the expression for output X.

X = (HG + I) (DEF) + (A+B) C



e. (8 pts) Give the truth table for the following transistor level schematic. Explain the source of 'good' logic 0's and 1's (using the labels P1, P2, N1 and N2) under each of the four input combinations.



A	B	P1	N1	P2	N2	OUT1	OUT
0	0	ON (S)	OFF	OFF	OFF	1	O (S)
0	1	ON (W)	OFF	ON	ON	A	A' (S)
1	0	OFF	ON(S)	OFF	OFF	O	1 (S)
1	1	OFF	ON(W)	ON	ON	A	A'(S)

Question3 (18 pts.): A majority gate with three inputs signals logic one on its output if two or more of its inputs are one, and zero otherwise. A minority gate is its complement.

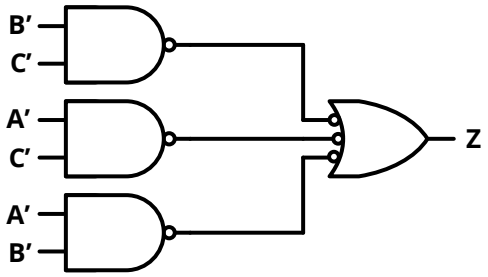
a. (2 pts) Give the boolean equation for a minority gate as a sum of products.

a	b	c	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Z: a \ bc	00	01	11	10
0	1	1	0	1
1	1	0	0	0

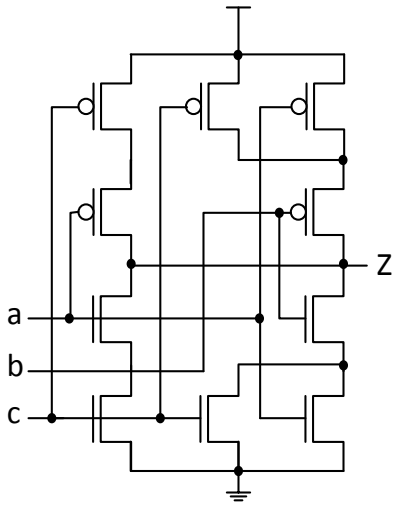
Z=b'c'+a'c'+a'b'

b. (4 pts) Sketch the circuit diagram for a minority gate using NAND gates and inverters.



c. (10 pts) Sketch the transistor-level circuit diagram for an alternative implementation as a single stage of CMOS logic.

Z=b'c'+a'c'+a'b'=b'(c'+a')+a'c'=[(b+ac).(a+c)]'=[b.(a+c)+ac]' (lower N network)
Taking DeMorgan's: Z = b'.(a'+c')+a'c' (upper P network)



d. (2 pts) Calculate the number of transistors required for each implementation.

Gate Level Implementation :	**Transistor Level Implementation:**
NAND gate = 4 transistors,	**5 PMOS transistors (PUN)**
3 NAND gates = 12 transistors.	**5 NMOS transistors (PDN)**
Inverter = 2 transistors,	
3 Inverters = 6 transistors.	
OR gate = 6 transistors	
Total = 24 transistors	**Total = 10 transistors**

Question4 (24 pts.):

a. (10 pts) Explain each parth of the VHDL code given below. What function does this code implements?

```
entity my_logic is
--Entity defines two inputs clock and data
--one output LED which is 8 bits, this circuit is
sequential (CLK)
    Port ( CLK, D : in  STD_LOGIC;
           LED : out STD_LOGIC_VECTOR(7 downto 0));
end my_logic;
-- 2 signals register and clock divider (5 bit)
architecture Behavioral of my_logic is
    signal clock_div : STD_LOGIC_VECTOR(4 downto 0);
    signal my_reg : STD_LOGIC_VECTOR(7 downto 0) := X"00";
begin
-- synchronous with clock
    process (CLK)
    begin
-- generate new clock
        if (CLK'event and CLK = '1') then
            clock_div <= clock_div + '1';
        end if;
    end process;
-- based on new clock shift bits to the right
    process (clock_div(4))
    begin
        if (clock_div(4)'event and clock_div(4) = '1') then
            my_reg (7) <= D;
            my_reg (6) <= my_reg (7);
            my_reg (5) <= my_reg (6);
```

```
            my_reg (4) <= my_reg (5);
            my_reg (3) <= my_reg (4);
            my_reg (2) <= my_reg (3);
            my_reg (1) <= my_reg (2);
            my_reg (0) <= my_reg (1);
        end if;
    end process;
-- turn on each led when d is shifted through
    LED <= my_reg;
end Behavioral;
```

This is a shift register!

b. (14 pts) An internal behaviour of priority encoder is defined by the truth table below. Write a complete, commented VHDL code that implements the following function specified.

Inputs				Output		
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

```
VHDL Code:
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY priority IS
       PORT ( d       : IN    STD_LOGIC_VECTOR(3 DOWNTO 0) ;
                      a       : OUT   STD_LOGIC_VECTOR(1 DOWNTO 0) ;
                      v       : OUT   STD_LOGIC ) ;
END priority ;
ARCHITECTURE Behavior OF priority IS
BEGIN
       a <=    "11" WHEN w(3) = '1' ELSE
               "10" WHEN w(2) = '1' ELSE
               "01" WHEN w(1) = '1' ELSE
               "00" ;
       v <= '0' WHEN w = "0000" ELSE '1' ;
END Behavior ;
```

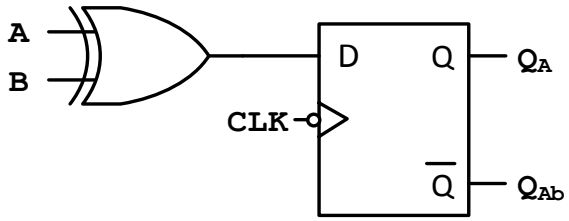
```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY priority IS
       PORT ( d       : IN    STD_LOGIC_VECTOR(3 DOWNTO 0) ;
```

```
                        a       : OUT   STD_LOGIC_VECTOR(1 DOWNTO 0) ;
                        v       : OUT   STD_LOGIC ) ;
END priority ;
ARCHITECTURE Behavior OF priority IS
BEGIN
        PROCESS ( d )
        BEGIN
                IF d(3) = '1' THEN
                        a <= "11" ;
                ELSIF d(2) = '1' THEN
                        a <= "10" ;
                ELSIF d(1) = '1' THEN
                        a <= "01" ;
                ELSE
                        a <= "00" ;
                END IF ;
        END PROCESS ;
        v <= '0' WHEN d = "0000" ELSE '1' ;
END Behavior ;
```

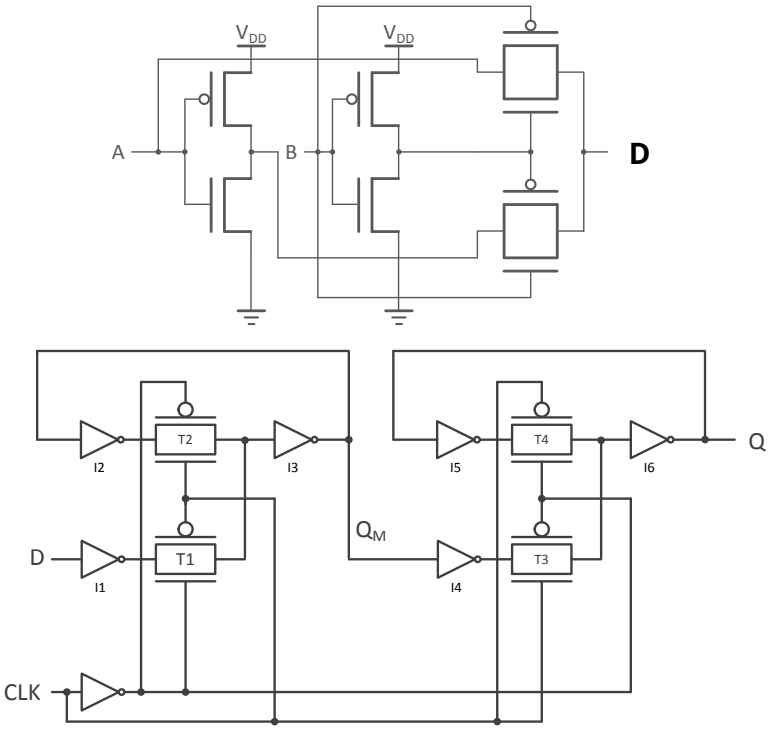
```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY priority IS
        PORT ( d        : IN    STD_LOGIC_VECTOR(3 DOWNTO 0) ;
                        a       : OUT   STD_LOGIC_VECTOR(1 DOWNTO 0) ;
                        v       : OUT   STD_LOGIC ) ;
END priority ;
ARCHITECTURE Behavior OF priority IS
BEGIN
        PROCESS ( d )
        BEGIN
                a <= "00" ;
                IF d(1) = '1' THEN a <= "01" ; END IF ;
                IF d(2) = '1' THEN a <= "10" ; END IF ;
                IF d(3) = '1' THEN a <= "11" ; END IF ;
                z <= '1' ;
                IF d = "0000" THEN v <= '0' ; END IF ;
        END PROCESS ;
END Behavior ;
```

Question5 (20 pts.):

Consider the sequential circuit given below.



a. (14 pts) Implement the given function to transistor-level schematic diagram for static CMOS logic. Label all the inputs, outputs and global ports.



b. (6 pts) Using the inputs and outputs given above, derive the truth table and the timing waveform.

A	B	DA	CLK	QA
0	0	0	↓	0
0	1	1	↓	1
1	0	1	↓	1
1	1	0	↓	0