EASTERN MEDITERRANEAN UNIVERSITY
Faculty of Engineering
Department of Electrical and Electronic Engineering

EENG 115/INFE115 Course Description

Semester	Spring 2019-20	**Pre-requisite**: -	**Credit Hrs.** : 4
Instructors	Prof. Dr. Mustafa Kemal Uyguroğlu	mustafa.uyguroglu@emu.edu.tr	
	Assist. Prof. Dr. Hassan AbouRajab	Hassan.rajab@emu.edu.tr	

Catalog Description:

Number systems, arithmetic operations, decimal codes, alphanumeric codes, Boolean algebra, Karnaugh maps, NAND and NOR gates, exclusive-OR gates, integrated circuits, combinational circuits, decoders, encoders, multiplexers, adders, subtractors, multipliers, sequential circuits, latches, flip-flops, sequential circuits analysis, registers, counters, RAM and ROM memories, programmable logic technologies (PLA, PLD, CPLD, FPGA).

Prerequisite by Topic: Basic knowledge of some algebraic structures and their properties.

Textbook: M. M. Mano, M. D. Ciletti, Digital Design (Fourth Edition), Prentice-Hall 2007.

References:

Fredrick J. Hill & Gerald R. Peterson, Introduction to Switching Theory & Logical Design, John Wiley & Sons 1981

Thomas L. Floyd, Digital Fundamentals , Merrill, imprint of Macmillan Publishing Company New York, 1994.

M. M. Mano & C. R. Kime, Logic and Computer Design Fundamentals, Prentice-Hall 2001.

B. Stephen & V. Zvonko, Fundamentals of Digital Logic with VHDL Design with CD-ROM, McGraw-Hill 2000

Course Objectives : A student who successfully fulfills the course requirements will have demonstrated an ability to

- Perform artihmetic operaions in many number sytems
- Manipulate Boolean algebraic structures
- Analyze and design various combinational logic circuits
- Anlayze and design clocked sequential circuits

Open Office Hours : First try to solve your problem yourself, failing, ask a friend, if this fails ask a second friend and if unsuccessful come as a group of three to see me at any time with your problem and a rough attempt to a solution and you will be seen A.S.A.P.

COURSE OUTLINE & ORGANIZATION

WK #	HRS	DESCRIPTION
1-2	8	Binary systems: Digital circuits, number systems, arithmetic operations, decimal codes, alphanumeric Codes.
3-5	10	Boolean algebra and logic gates: Axiomatic definition of Boolean algebra, theorems and properties of Boolean algebra, canonical and standard forms of Boolean functions, other logic operations, digital logic gates, integrated circuits.
5-7	8	Simplification of Boolean functions: The map method, prime implicants, product of sums simplification, two-level NAND and NOR implementations, other two-level
8	4	Logic Implementations: multilevel NAND and NOR circuits, the tabulation method, Exclusive-OR function
9		Midterm Exam
10	4	Multilevel NAND and NOR circuits, the tabulation method, Exclusive-OR function
11-13	12	Combinational Logic: Analysis procedure, design procedure, code conversion, binary adder-sub tractor, 4-bit parallel adder-subtractor, carry propagation, look-ahead carry generation, decimal adder.
14-15	10	MSI components: magnitude comparator, decoders and encoders, priority encoders, multiplexers, combinational logic implementation.
16-17	8	Synchronous sequential circuits: Flip-flops, triggering of flip-flops, analysis of clocked sequential circuits, state reduction and assignment, flip-flop excitation tables, design procedure, design of counters.
18-19		FINAL EXAMS

Design Component:

Engineering Science Credit: 3

Engineering Design Credit: 1

Laboratory/Studio Works:
Laboratory sessions are organized in parallel to theoretical study given in classrooms. Students perform at least 6 different experiments and submit reports for evaluation.

GRADING SYSTEM

Midterm Exam	25%
Quizzes	15%
Lab	15%
Homeworks	10%
Final	35%

NG Policy:
Attendance to the classes is compulsory. All students who receive a failing final grade and attend the classes less than 60% will receive the grade NG.

Make-Up Examination Policy:
Students missing an examination should provide a valid excuse within three days following the examination they missed. No separate make-up exams are administered for midterm and final exams. Re-sit examination are administered as make-up examinations, instead.
Students who fail to attend less than 60% of classes will not be given Make-up examination.