Faculty of Engineering

DEPARTMENT of ELECTRICAL AND ELECTRONIC ENGINEERING

EENG (INFE)115 Introduction to Logic Design

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Final EXAMINATION

January 05, 2017

Duration : 120 minutes

Number of Questions: 4

Good Luck

STUDENT'S	
NUMBER	
NAME	SOLUTIONS
SURNAME	
GROUP NO	

Question		**Points**
1		30
2		30
3		30
4		30
TOTAL		**120**

Read the following instructions carefully:

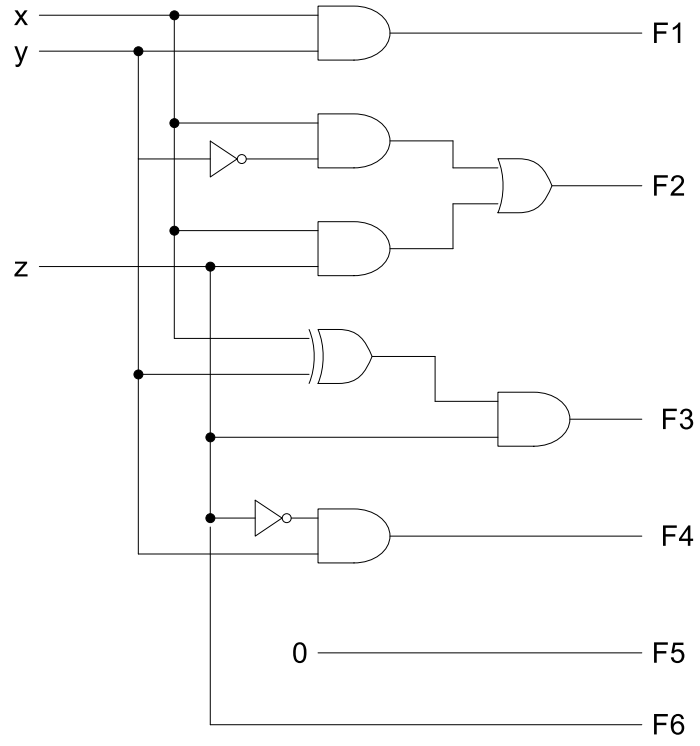
1. **Calculators** are not allowed.
2. Switch off **mobile phones** and **do not borrow** any stationery from your friends.
3. In your solutions, **show all details** you claim credit for.

Question 1

Design a **combinational circuit** that accepts a **three** bit number and generates an **output** binary number equal to the **square of the input.**

Inputs			Outputs					
x	y	z	F1	F2	F3	F4	F5	F6
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

F6=z
F5=0
F4=x'yz'+xyz'=yz'
F3=x'yz+xy'z=(x⊕y)z
F2=xy'+xz
F1=xy

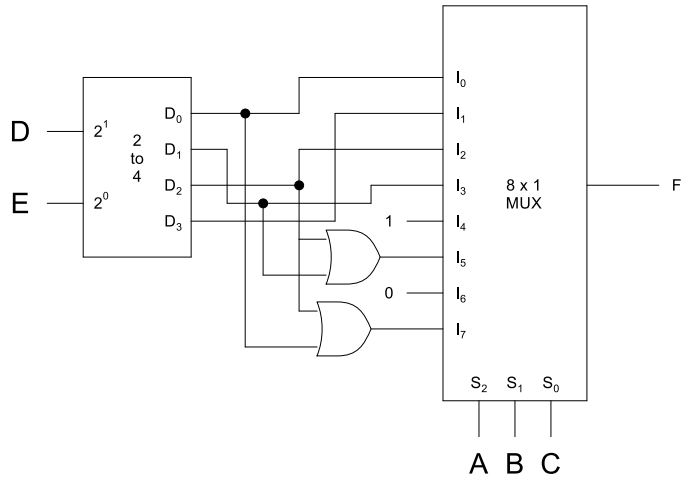


Question 2

Implement the following Boolean function with a 8×1 **multiplexer**, a **2-to-4-line decoder** and two **2-input OR** gates. Note that the complement inputs are not available.

$$F\left(A,B,C,D,E\right)=\sum\left(0,7,10,13,16,17,18,19,21,22,28,30\right)$$

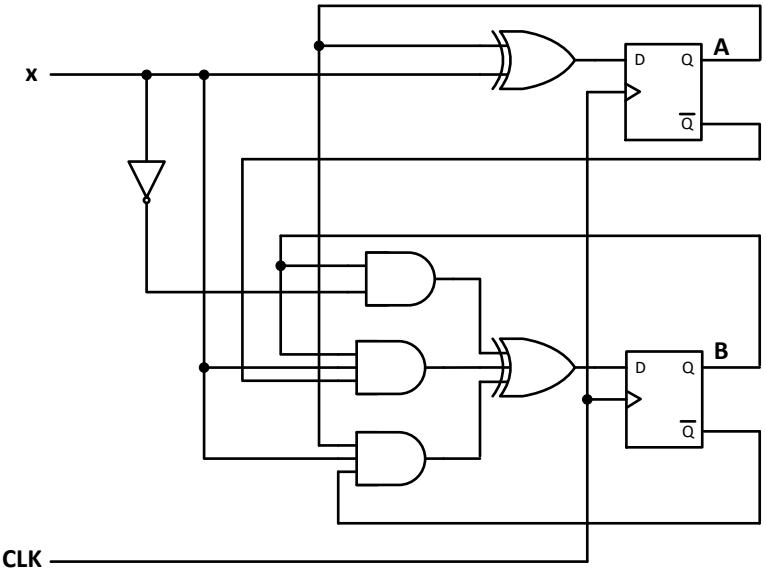
S_2	S_1	S_0	Inputs		Output	
A	B	C	D	E	F	
0	0	0	0	0	1	I_0 =D'E'
0	0	0	0	1	0	
0	0	0	1	0	0	
0	0	0	1	1	0	
0	0	1	0	0	0	I_1 = DE
0	0	1	0	1	0	
0	0	1	1	0	0	
0	0	1	1	1	1	
0	1	0	0	0	0	I_2 = DE'
0	1	0	0	1	0	
0	1	0	1	0	1	
0	1	0	1	1	0	
0	1	1	0	0	0	I_3 = D'E
0	1	1	0	1	1	
0	1	1	1	0	0	
0	1	1	1	1	0	
1	0	0	0	0	1	I_4 = 1
1	0	0	0	1	1	
1	0	0	1	0	1	
1	0	0	1	1	1	
1	0	1	0	0	0	I_5 = D'E+DE'
1	0	1	0	1	1	
1	0	1	1	0	1	
1	0	1	1	1	0	
1	1	0	0	0	0	I_6 = 0
1	1	0	0	1	0	
1	1	0	1	0	0	
1	1	0	1	1	0	
1	1	1	0	0	1	I_7 = C'D'+CD'
1	1	1	0	1	0	
1	1	1	1	0	1	
1	1	1	1	1	0	


D
E
2^1
2^0
2 to 4
D_0
D_1
D_2
D_3
1
0
I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
8 x 1 MUX
F
S_2 S_1 S_0
A B C

Question 3

Mod-4 counter is a sequential circuit that has two flip-flops A and B and one input x. It consists of a combinatorial logic connected to the D flip-flops, as shown in Figure below. Analyze the circuit:

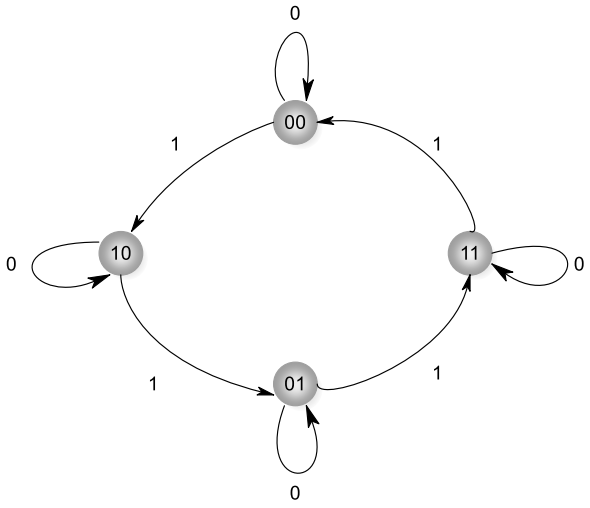
a) Derive the next state and output equations.
b) Derive the state table of the sequential circuit.
c) Draw the corresponding state diagram.



$$\underbrace{A(t+1)}_{\text{next state}} = D_A = \underbrace{A(t)}_{\text{present state}} \oplus x$$

$$B(t+1) = D_B = \left(B(t)x'\right) \oplus \left(A'(t)B(t)x\right) \oplus \left(A(t)B'(t)x\right)$$

Present State		Input	Next State	
A	B	x	A	B
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	0	0

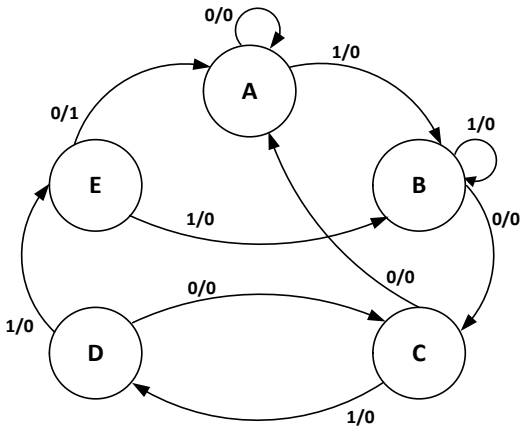


Question 4

The state diagram of a sequence detector which allows overlap is shown below. A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. In a sequence detector that allows overlap, the final bits of one sequence can be the start of another sequence. Using the state diagram given below and an input sequence **10110**:

a) Assign binary values to the states and derive the state table.
b) Derive the **simplified** state equations.
c) Use **JK flip-flops** and design a synchronous sequence detector circuit.
d) Is this a **Mealy** or **Moore** model?

Treat unused states as don't care conditions.



State	Assignment
A	000
B	001
C	010
D	011
E	100

Present State			Input	Next State			Output	Flip-flops Inputs					
A	B	C	x	A	B	C	y	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	0	0	0	X	0	X	0	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X
0	0	1	0	0	1	0	0	0	X	1	X	X	1
0	0	1	1	0	0	1	0	0	X	0	X	X	0
0	1	0	0	0	0	0	0	0	X	X	1	0	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X
0	1	1	0	0	1	0	0	0	X	X	0	X	1
0	1	1	1	1	0	0	0	1	X	X	1	X	1
1	0	0	0	0	0	0	1	X	1	0	X	0	X
1	0	0	1	0	0	1	0	X	1	0	X	1	X
1	0	1	0				X	X	X	X	X	X	X
1	0	1	1				X	X	X	X	X	X	X
1	1	0	0				X	X	X	X	X	X	X
1	1	0	1				X	X	X	X	X	X	X
1	1	1	0				X	X	X	X	X	X	X
1	1	1	1				X	X	X	X	X	X	X

AB \ Cx	00	01	11	10
00				
01			1	
11	x	x	x	x
10	x	x	x	x

$J_A=BCx$

AB \ Cx	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	x	x	x	x
10	1	1	x	x

$K_A=1$

AB \ Cx	00	01	11	10
00				1
01	x	x	x	x
11	x	x	x	x
10	0	0	x	x

$J_B=Cx'$

AB \ Cx	00	01	11	10
00	x	x	x	x
01	1	0	1	0
11	x	x	x	x
10	x	x	x	x

$K_B = C'x' + Cx$

AB \ Cx	00	01	11	10
00		1	x	x
01		1	x	x
11	x	x	x	x
10	0	1	x	x

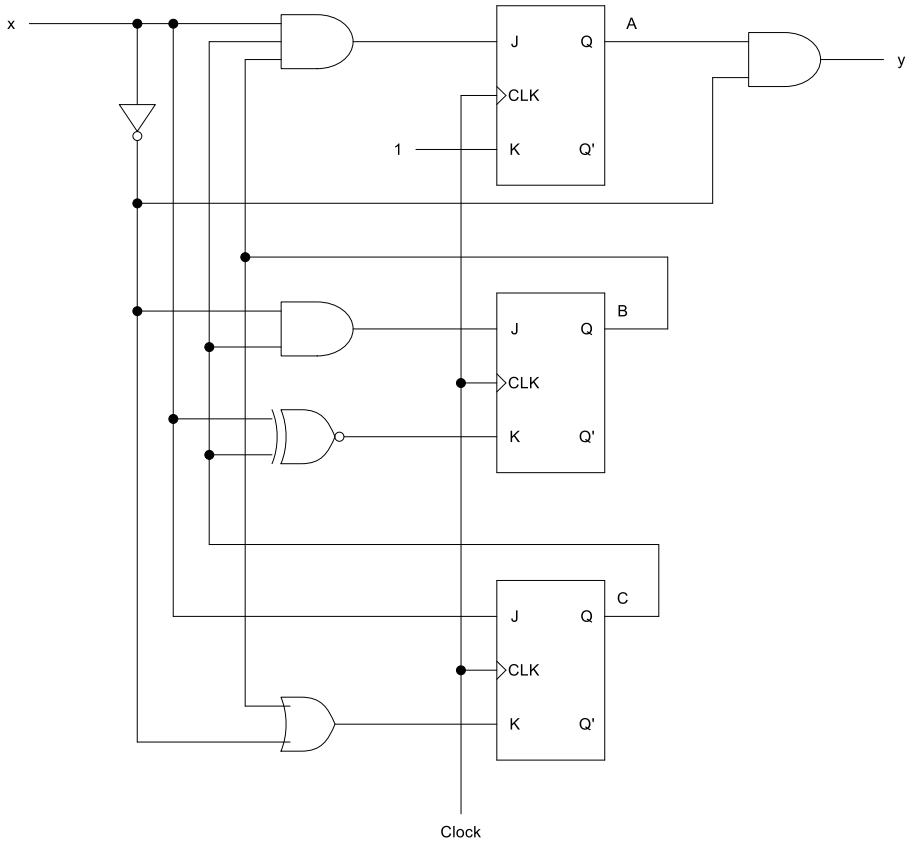
$J_C = x$

AB \ Cx	00	01	11	10
00	x	x		1
01	x	x	1	1
11	x	x	x	x
10	x	x	x	x

$K_C = B + x'$

AB \ Cx	00	01	11	10
00				1
01			1	
11	x	x	x	x
10	1	0	x	x

$Y = Ax'$


x
J
Q
A
CLK
1
K
Q'
y
B
C
Clock