Faculty of Engineering

DEPARTMENT of ELECTRICAL AND ELECTRONIC ENGINEERING

EENG (INFE) 115	Instructor:
Introduction to Logic Design	G. YEMİŞÇİOĞLU
Final EXAMINATION	Duration: 120 minutes
June 12, 2017	Number of Questions: 4

Good Luck

STUDENT'S	
NUMBER	SOLUTIONS
NAME	
SURNAME	
GROUP NO.	

Question	Achieved	Points
1		30
2		30
3		30
4		30
TOTAL		120

Read the following instructions carefully:

1. Calculators are not allowed.
2. Switch off mobile phones and do not borrow any stationery from your friends.
3. In your solutions, show all details you claim credit for.

Question 1:

Design a **combinational circuit** that accepts a **four-bit** number **(A,B,C,D)** and generates an output which is equal to the **sum of the binary numbers formed by the input (AB) and (CD)**.
(**30 pts**)

AB + CD = ??

	Inputs			Outputs		
A	**B**	**C**	**D**	**x**	**y**	**z**
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

x (A,B,C,D) = Σ(7, 10, 11, 13, 14, 15)
y (A,B,C,D) = Σ(2, 3, 5, 6, 8, 9, 12, 15)
z (A,B,C,D) = Σ(1, 3, 4, 6, 9, 11, 12, 14)

x'sK-MAP

CD / AB	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	1	1	1
10	0	0	1	1

x = AC + ABD + BCD

y'sK-MAP

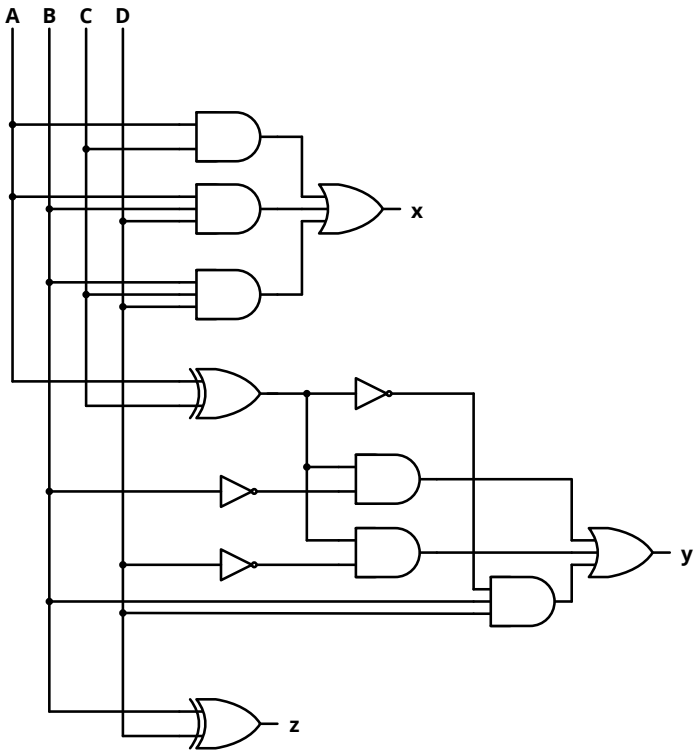
CD / AB	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	1	0	1	0
10	1	1	0	0

y = AC'D' + AB'C' + A'B'C + A'CD' + A'BC'D + ABCD
y = AC'D' + A'CD' + AB'C' + A'B'C + A'BC'D + ABCD
y = D' (AC' + A'C) + B' (AC' + A'C) + BD (A'C' + AC)
y = D' (A ⊕ C) + B' (A ⊕ C) + BD (A ⊕ C)'

z'sK-MAP

CD / AB	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	0	0	1
10	0	1	1	0

z = BD' + B'D



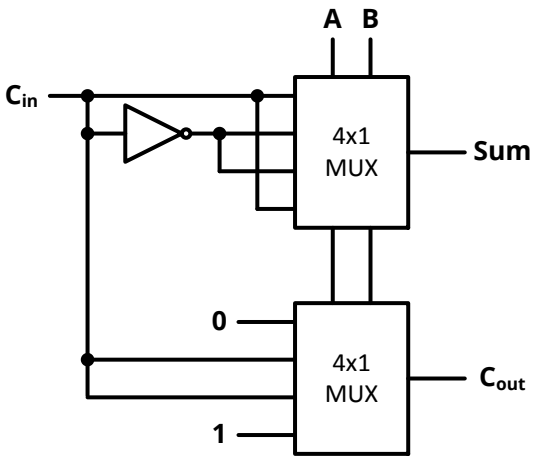
Question 2:

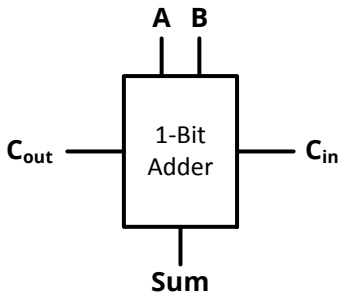
a) Implement a 1-bit full adder circuit by using 4 x 1 Multiplexer and an inverter.
b) Construct 4-bit ripple carry adder using 1-bit full adder implemented in (a).
c) Implement a 4-bit BCD adder using (b) to add two BCD digits. Make sure that the circuit also detects invalid BCD digits and generates the correct BCD output sum.

(30 pts)

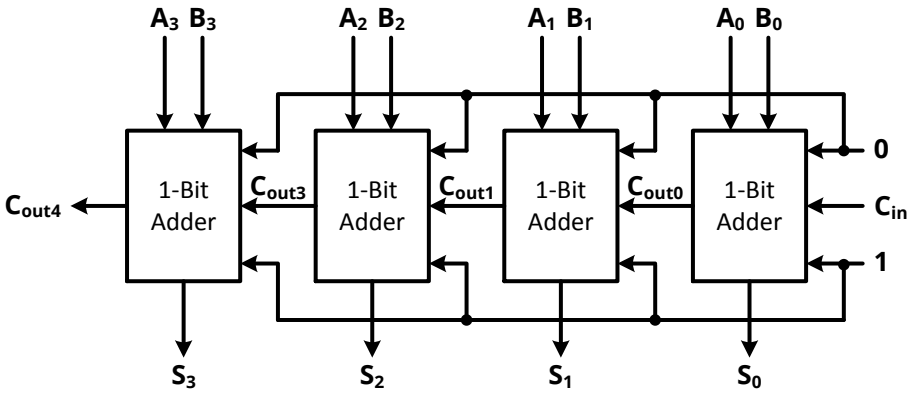
a) (10 pts)

A	B	C_{in}	C_{out}	Mux 1 IN	Sum	Mux 2 IN
0	0	0	0	0	0	C_{in}
0	0	1	0		1	
0	1	0	0	C_{in}	1	C_{in}'
0	1	1	1		0	
1	0	0	0	C_{in}	1	C_{in}'
1	0	1	1		0	
1	1	0	1	1	0	C_{in}
1	1	1	1		1	





b) (5 pts)



c) (15 pts)

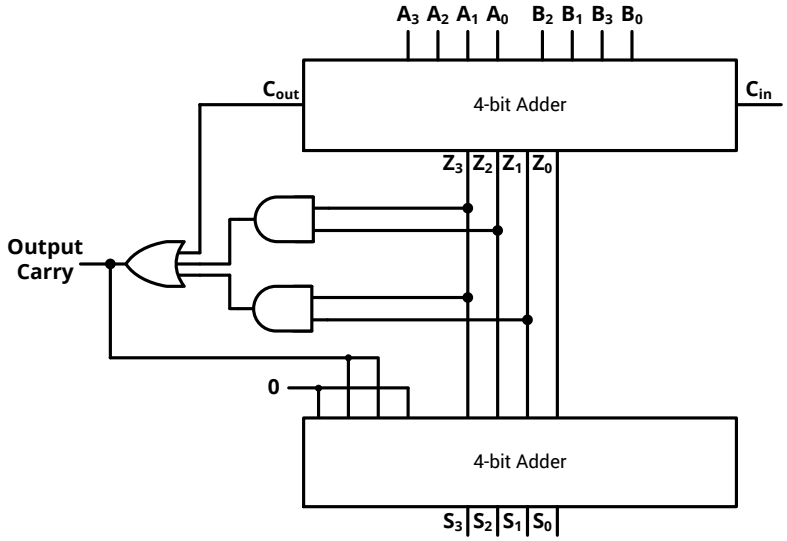
Z3	Z2	Z1	Z0	Error
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Error's K-MAP

Z_3Z_2 \ Z_1Z_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

$$Err = Z_3Z_2 + Z_3Z_1$$

$$Output\ Carry = C_{out} + Z_3Z_2 + Z_3Z_1$$

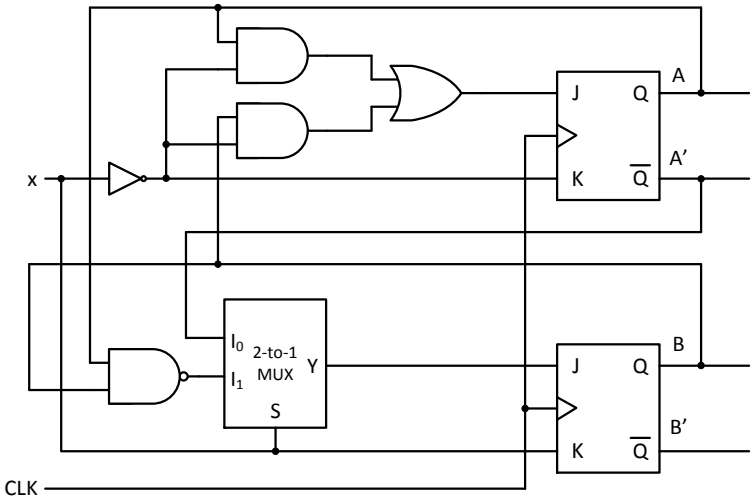


Question 3:

Sequential circuit shown below has two flip-flops A and B and one input x. It consists of a combinatorial logic connected to the flip-flops, as shown in Figure below. Analyse the circuit:

a) Derive the next state equations.
b) Derive the state table of the sequential circuit.
c) Draw the corresponding state diagram.

(**30 pts**)



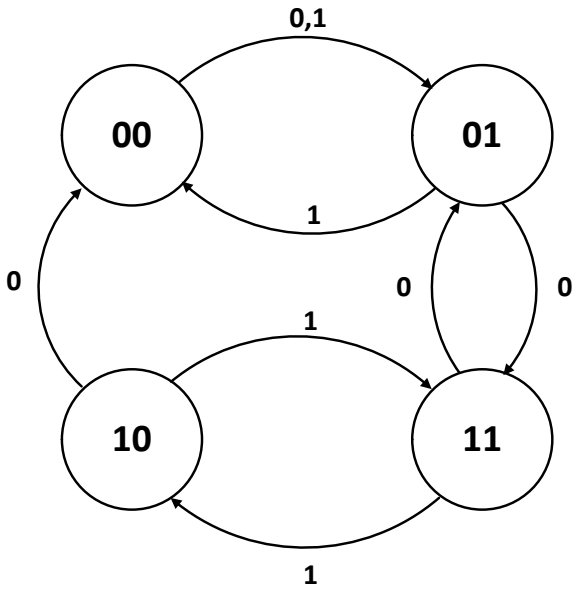
a) (10 pts)

$J_A = A.x' + B.x'$	$K_A = x'$	$J_B = A'.x' + (A.B)'x$ $J_B = A'.x' + (A' + B')x$ $J_B = A'.x' + A'x + B'.x$ $J_B = A'(\cancel{x' + x}) + B'.x$ $J_B = A' + B'.x$	$K_B = x$
$A(t+1) = J_A.A' + K_A'.A$ $A(t+1) = (A.x' + B.x')A' + (x')'A$ $A(t+1) = \cancel{A'.A.x'} + A'.B.x' + Ax$ $A(t+1) = A'.B.x' + Ax$		$B(t+1) = J_B.B' + K_B'.B$ $B(t+1) = (A'+B'.x)B' + B.x'$ $B(t+1) = A'B' + B'.B'x + B.x'$ $B(t+1) = A'B' + B'x + Bx'$ $B(t+1) = A'B' + B \text{ XOR } x$	

b) (10 pts)

Present		Input	Next	
A	**B**	**x**	**A**	**B**
0	0	0	0	1
0	0	1	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	0

c) (10 pts)



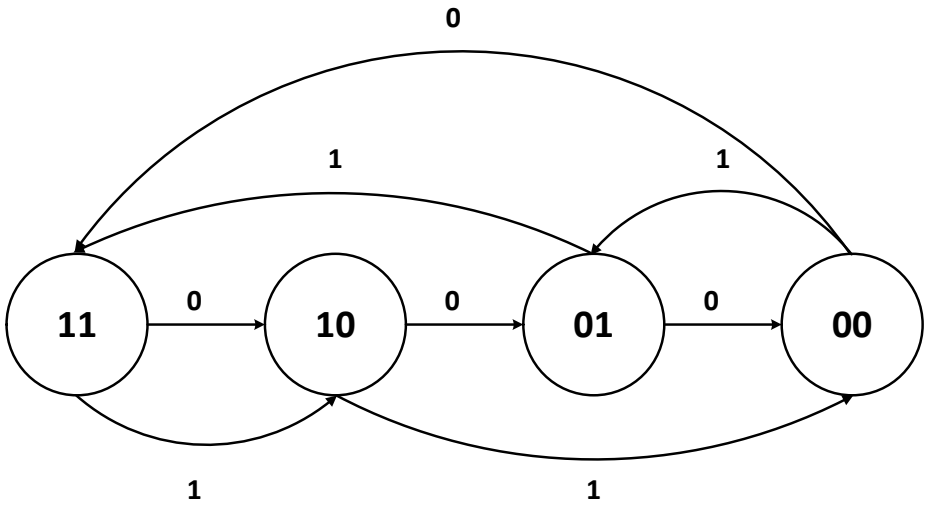
Question 4:

Design a **2-bit** counter using **JK-Flip flops** with one input. When the input is **0**, the counter counts down, with the repeated sequence **(11-10-01-00)**. When the input is **1**, the counter counts repeated random sequence **(00-01-11-10).**

a) Draw a state diagram for the sequential circuit.
b) Derive the state table for the sequential circuit.
c) Derive the simplified flip flops input equations.
d) Draw the logic circuit diagram of a 2-bit counter.

(**30 pts**)

a) (7.5 pts)



b) (7.5 pts)

Step1: Characteristic and Excitation Table of JK-Flip Flop

Characteristic			Excitation			
J	K	Q	Q(t)	Q(t+1)	J	K
0	0	Q	0	0	0	X
0	1	0	0	1	1	X
1	0	1	1	0	X	1
1	1	Q’	1	1	X	0

Step2: Stata Table

Present State		Input	Next State		Flip-Flops Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X	1	X
0	0	1	0	1	0	X	1	X
0	1	0	0	0	0	X	X	1
0	1	1	1	1	1	X	X	0
1	0	0	0	1	X	1	1	X
1	0	1	0	0	X	1	0	X
1	1	0	1	0	X	0	X	1
1	1	1	1	0	X	0	X	1

c) (7.5 pts)

JA's K-MAP

A \ Bx	00	01	11	10
0	1	0	1	0
1	X	X	X	X

JA = B'x' + Bx

KA's K-MAP

A \ Bx	00	01	11	10
0	X	X	X	X
1	1	1	0	0

KA = B'

JB's K-MAP

A \ Bx	00	01	11	10
0	1	1	X	X
1	1	0	X	X

JB = A' + x'

KB's K-MAP

A \ Bx	00	01	11	10
0	X	X	0	1
1	X	X	1	1

KB = A + x'

d) (7.5 pts)