Faculty of Engineering

ELECTRICAL AND ELECTRONIC ENGINEERING DEPARTMENT

EENG115 / INFE115 Introduction to Logic Design

EENG211 / INFE211 Digital Logic Design I

Fall 2009-10

Instructors:

M. K. Uyguroğlu

H. Demirel

Final EXAMINATION

Jan. 13, 2010

Duration : 120 minutes

Number of Problems: 8

Good Luck

STUDENT'S	
NUMBER	
NAME	
SURNAME	
GROUP NO	

Problem	Achieved	Maximum
1		10
2		10
3		15
4		15
5		10
6		15
7		15
8		15
TOTAL		105

Question 1 (10 points)

Answer the following questions regarding Boolean algebra.

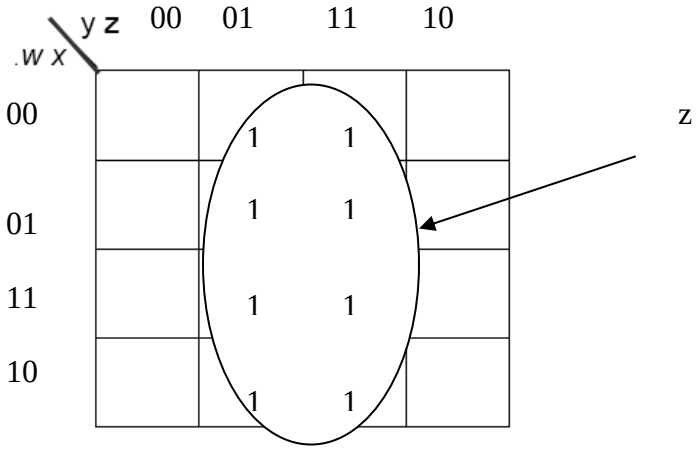
a) Minimize the function F(w,x,y,z) using algebraic modifications. Show the result as a sum of products with a minimum number of literals. (6 points)

F(w,x,y,z) = (y'+wy'(xz+xz'))z + (xy'+(x+y)'+z')'+ y(z+wx'(w'+z))
=[y` +wy`x]z + (xy` +x`y` + z`)` + y(z + wx`z)
= y`z + wxy`z + (y` + z`)` + y (z)
= y`z (1 + wx) + yz + yz
= y`z + yz
= z

Algebraically minimized F = z

b) Convert the original function F(w,x,y,z) from part a) to a sum-of-product form and minimize it using Karnaugh map. Compare the results. (4 points)

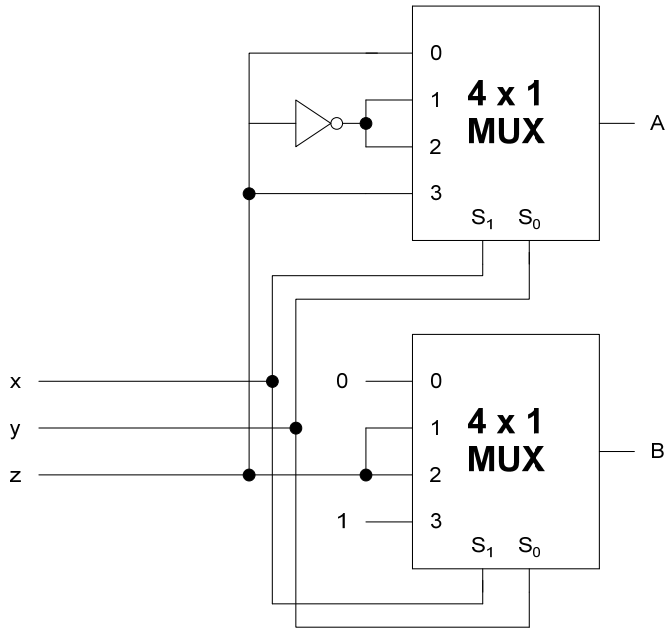
F(w,x,y,z) = (y'+wy'(xz+xz'))z + (xy'+(x+y)'+z')'+ y(z+wx'(w'+z))
=[y` +wy`x]z + (xy` +x`y` + z`)` + y(z + wx`z)
= y`z + wy`xz + yz + wx`yz



K-map minimized F = z

Question 2 (10 points):
Answer the following questions regarding combinational logic.

a) Determine the outputs functions *A* and *B* as sums of minterms. You may use any process to determine the result, but show your work. (7 points)



x	y	z	A	B	A	B
0	0	0	$I_0=z$	$I_0=0$	0	0
0	0	1			1	0
0	1	0	$I_1=z'$	$I_1=z$	1	0
0	1	1			0	1
1	0	0	$I_2=z'$	$I_2=z$	1	0
1	0	1			0	1
1	1	0	$I_3=z$	$I_3=1$	0	1
1	1	1			1	1

$$A = \sum(1,2,4,7)$$
$$B = \sum(3,5,6,7)$$

b) The circuit shown in a) has the functionality of a commonly used arithmetic component. What does the circuit do and what are other names for A and B? (3 points)
The circuit implements a FULL ADDER
A is the SUM
B is the CARRY……

Question 3 (15 points):

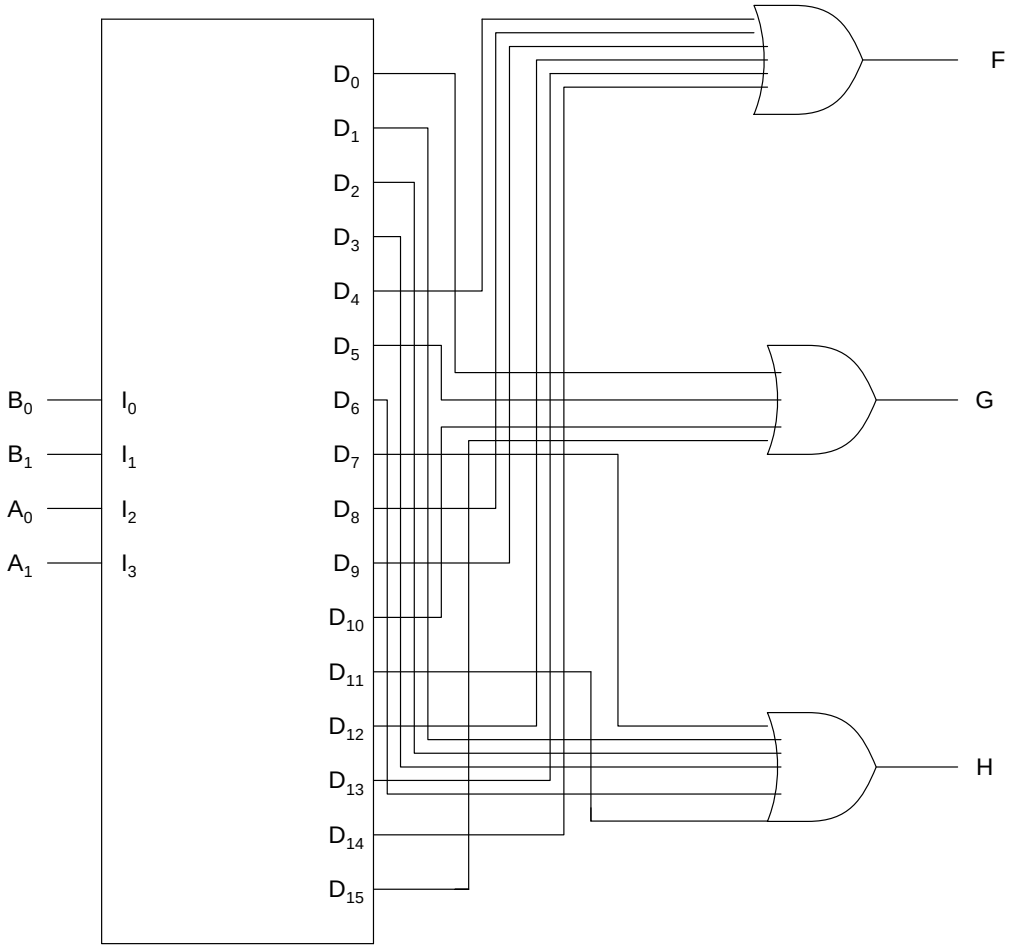
Design a magnitude comparator circuit for 2-bit binary numbers $A=A_1A_0$ and $B=B_1B_0$. The outputs are *F*, *G*, and *H*, where *F* is *1* if *A>B*, *G* is *1* if *A=B*, and *H* is *1* if *A<B*.

a) Fill in the truth table for the three outputs of the comparator and determine their function as sum of minterms. (9 points)

A_1	A_0	B_1	B_0	F(A>B)	G(A=B)	H(A<B)
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

$$F = \sum(4,8,9,12,13,14)$$
$$G = \sum(0,5,10,15)$$
$$H = \sum(1,2,3,6,7,11)$$

b) Implement your comparator design using a 4-to-16 line decoder shown below. (6 points)



Question 4 (15 points):
Answer the following questions regarding combinational logic design. Design a circuit (combinational, not sequential) that takes an unsigned 2-bit number, $X=X_1X_0$, and computes the square of that number, $Y=X^2$

a) How many outputs do you need? (2 points)

4

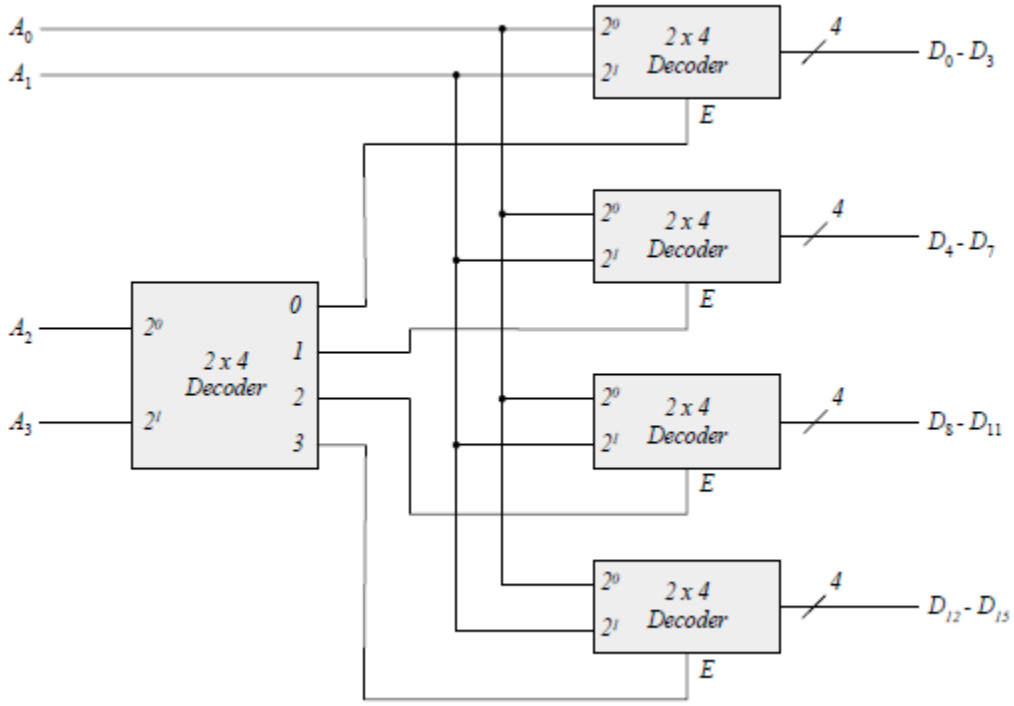
b) Show the truth table for this combinational circuit. Name the outputs Y_n, …, Y_1, Y_0 (with n depending on what you have determined in a). (10 points)

X_1	X_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	1	0	0
1	1	1	0	0	1

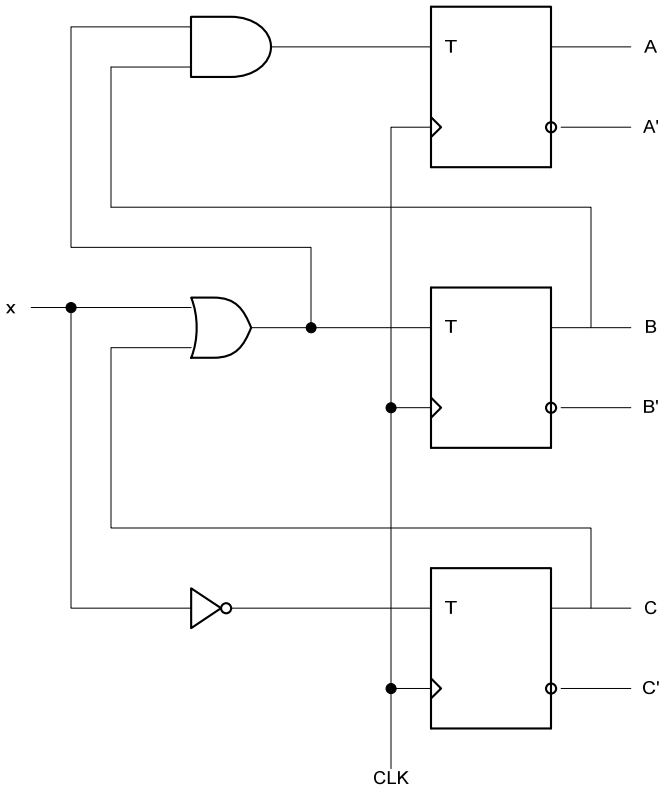
c) Determine the minimized output functions. (3 points)

$$Y_3 = X_1X_0$$
$$Y_2 = X_1X_0'$$
$$Y_1 = 0$$
$$Y_0 = X_0$$

Question 5 (10 points):
Design a 4-to-16-line decoder by using the minimum number of 2-to-4-line decoders. The 2-to-4-line decoders have an enable input ('1'=enabled) and the designed 4-to-16-line decoder does not have an enable. Name the inputs $A_0 \ldots A_3$ and the outputs $D_0 \ldots D_{15}$. Do not draw the internal circuit diagrams for the decoders.

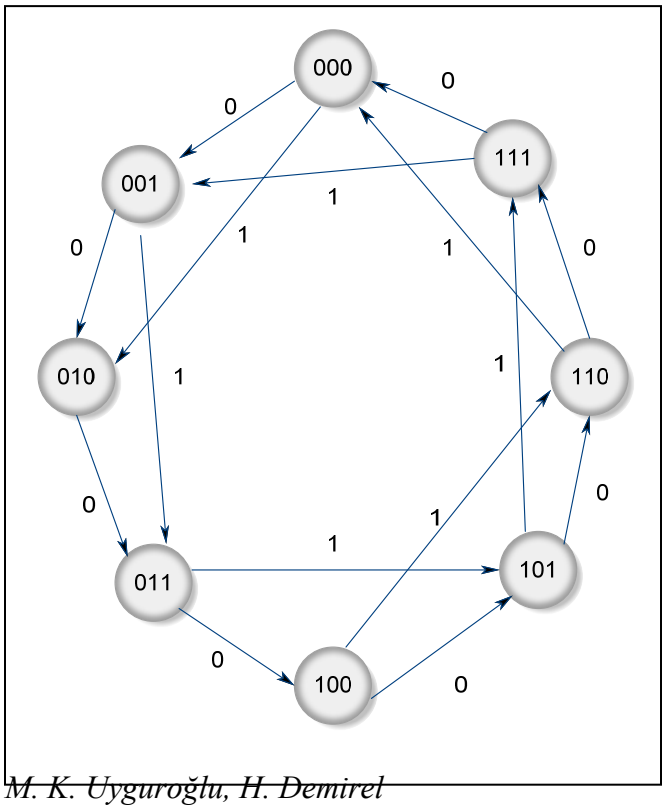


Question 6 (15 points):
Derive the state table and the state diagram of the sequential circuit shown below. Explain the function that the circuit performs.



$$T_A = B(C + x)$$
$$T_B = C + x$$
$$T_C = x'$$

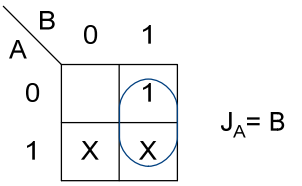
PS			in	NS			FF in		
A	B	C	x	A	B	C	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1	1
0	0	1	1	0	1	1	0	1	0
0	1	0	0	0	1	1	0	0	1
0	1	0	1	1	0	0	1	1	0
0	1	1	0	1	0	0	1	1	1
0	1	1	1	1	0	1	1	1	0
1	0	0	0	1	0	1	0	0	1
1	0	0	1	1	1	0	0	1	0
1	0	1	0	1	1	0	0	1	1
1	0	1	1	1	1	1	0	1	0
1	1	0	0	1	1	1	0	0	1
1	1	0	1	0	0	0	1	1	0
1	1	1	0	0	0	0	1	1	1
1	1	1	1	0	0	1	1	1	0



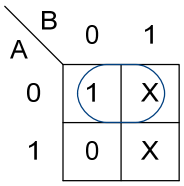
When x=0, it counts one by one and when x=1, it counts two by two.

Question 7 (15 points):
Use JK flip flops to design a counter with the repeated binary sequence:0,1,2.
The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

PS		NS		FF Inputs			
A	B	A	B	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X
1	1			X	X	X	X

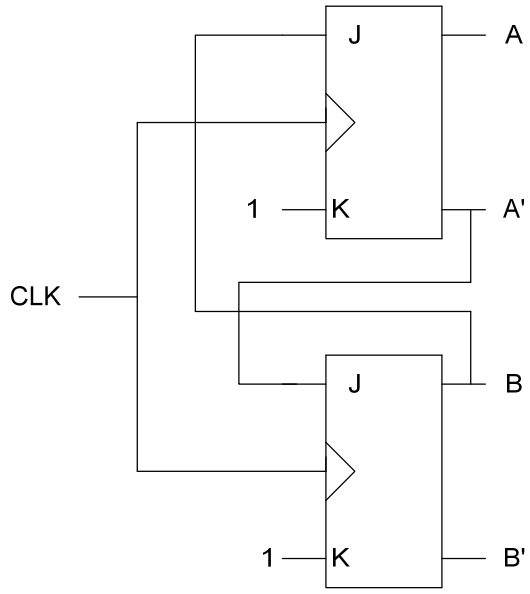


$J_A = B$



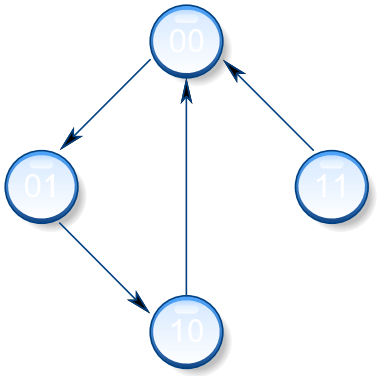
$J_B = A'$

$K_A = K_B = 1$

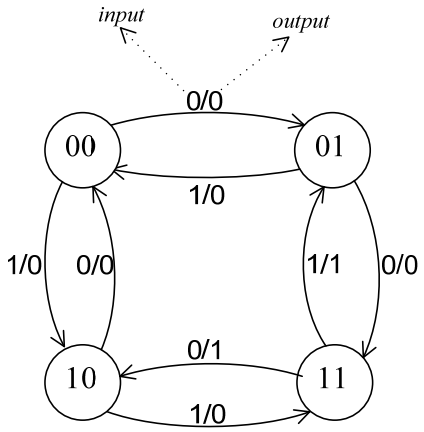


Analysis of circuit for unused state:

PS		NS		FF Inputs			
A	B	A	B	J_A	K_A	J_B	K_B
1	1	**0**	**0**	1	1	0	1



Question 8 (15 points):
Given the state diagram below, generate the state table and design a sequential circuit using D flip fops.



PS		In	NS		Out
A	B	x	A	B	y
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	0	1	0

Flip – Flop inputs

$D_A = A(t+1)$
$D_B = B(t+1)$
$Y = ABx'$

A \ Bx	00	01	11	10
0		1		1
1		1		1

A \ Bx	00	01	11	10
0	1			1
1		1	1	

$D_A = B'x + Bx' = B \oplus x$

$D_B = Ax + A'x' = (A \oplus x)'$