Faculty of Engineering
ELECTRICAL AND ELECTRONIC ENGINEERING DEPARTMENT

EENG211 / INFE211 Digital Logic Design I

Spring 2008-09

Instructor:
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Final EXAMINATION

June 11, 2009

Duration : 120 minutes

Number of Problems: 5

Good Luck

STUDENT'S	
NUMBER	
NAME	**SOLUTIONS**
SURNAME	
GROUP NO	

Problem		**Points**
1		20
2		20
3		20
4		20
5		25
TOTAL		105

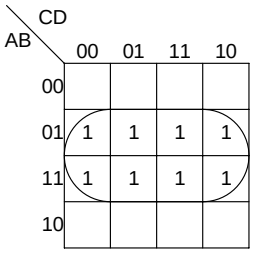
1. (a) What is -53 in 2's complement? (use 8 bits) [2.5 points]

53	2	1
26	2	0
13	2	1
6	2	0
3	2	1
1	2	1
0		

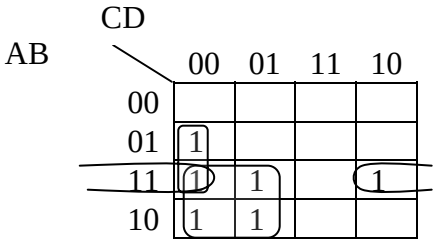
$53_{10} = (00110101)_2$
$-53_{10} = (11001011)_2$

(b) Express the following function as a product of maxterms:
f(A, B, C) = AB + C'A [5 points]
f(A,B.C)= ABC+ABC'+ABC'+AB'C'
$f(A,B,C) = \sum(4,6,7) = \prod(0,1,2,3,5)$

(c) Simplify the following Boolean expression to a minimum number of literals :
A'B(D' + C'D) + B(A + A'CD) [5 points]
=A'B((D'+C')(D'+D))+B((A+A')(A+CD))
=A'BC'+A'BD'+AB+BCD=B

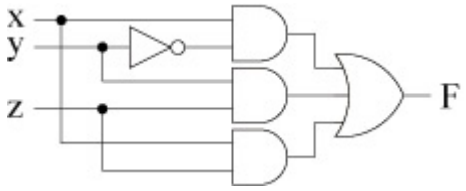


(d) Simplify the Boolean function represented in the following K-map: [2.5 points]



F(A,B,C,D)=AC'+ABD'+BC'D'

(e) Select the equivalent expression/s for the following logic gate structure: [5 points]



F=xy'+yz+xz

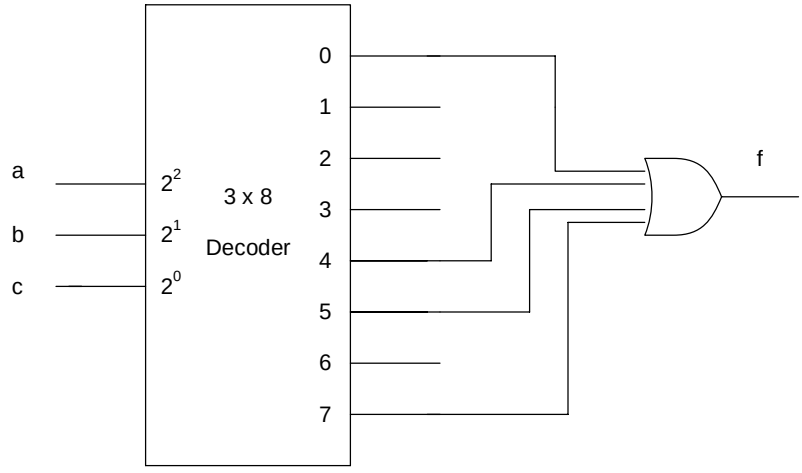
x \ yz	00	01	11	10
0			1	
1	1	1	1	

(a) F = x+yz
(b) F = xy'+yz
(c) F = xy'z + xy'z' + xyz + x'yz
(d) All of the above
(e) both (b) and (c)

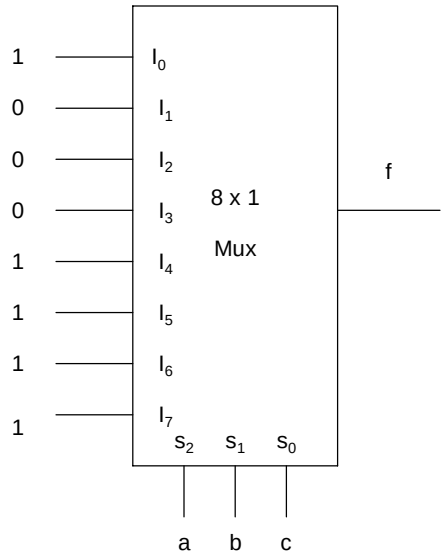
2. **Implement the truth table given below using**

Inputs			Output
a	**b**	**C**	**f**
0	0	0	1
0	0	1	0
0	1	0	Don't care
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Don't care
1	1	1	1

(a**) A single 3-to-8 Decoder and any simple logic gate (e.g. AND/OR/INV) [5 points]**

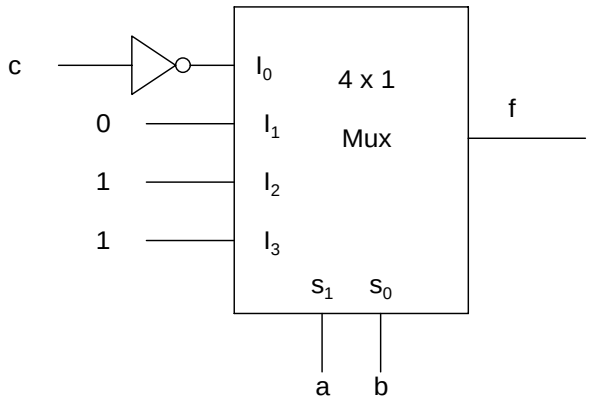


(b) A single 8-to-1 Multiplexer and any simple logic gate (e.g. AND/OR/INV) [5 points]

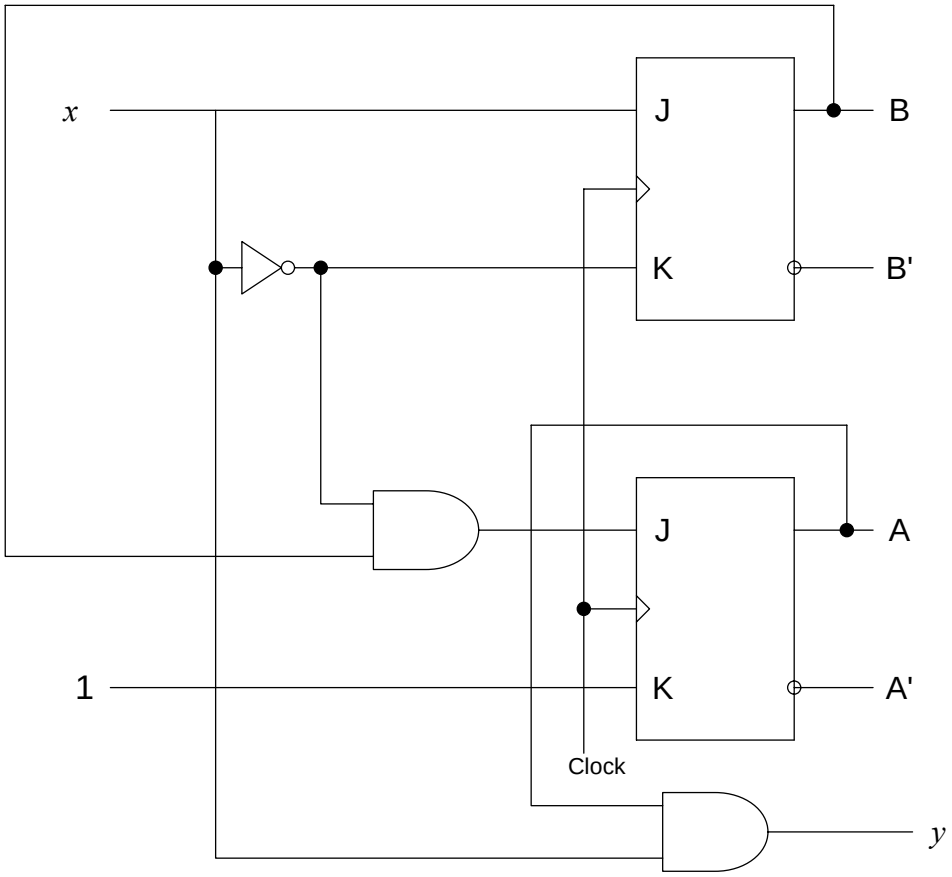


(c) A single 4-to-1 Multiplexer and any simple logic gate (e.g. AND/OR/INV) [10 points]

Inputs			Output
a	**b**	**C**	**f**
0	0	0	1
0	0	1	0
0	1	0	Don't care
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Don't care
1	1	1	1



3. **Here is a sequential circuit with one input *x* and one output *y*.**



(a) Derive the next state and output equations. [2 points]

$J_B = x$

$K_B = x'$

$J_A = Bx'$

$K_A = 1$

$y = Ax$

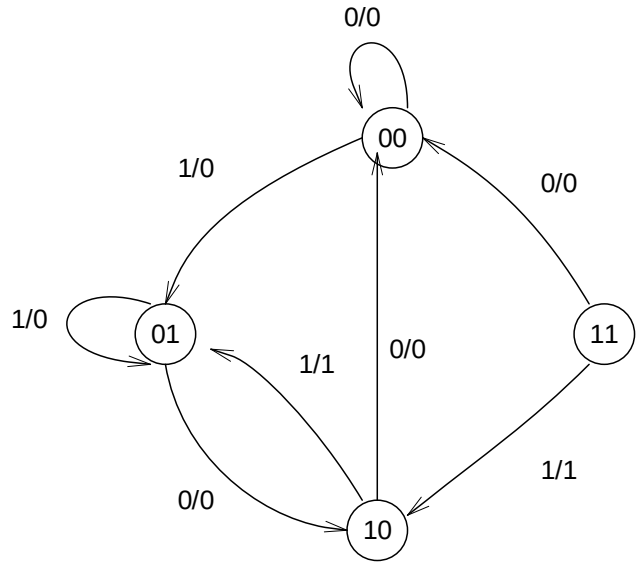
(b) Fill in the following characteristic table of JK-flip flop. [1 points]

J	**K**	**Q(*t*+1)**
0	**0**	**Q(t)**
0	**1**	**0**
1	**0**	**1**
1	**1**	**Q'(t)**

(c) The state table of the circuit: **[10 points]**

Present State		**Input**	**Next State**		**Output**	**Flip Flop Inputs**			
A	**B**	***x***	**A**	**B**	***y***	$\mathbf{J_A}$	$\mathbf{K_A}$	$\mathbf{J_B}$	$\mathbf{K_B}$
0	0	0	0	0	0	0	1	0	1
0	0	1	0	1	0	0	1	1	0
0	1	0	1	0	0	1	1	0	1
0	1	1	0	1	0	0	1	1	0
1	0	0	0	0	0	0	1	0	1
1	0	1	0	1	1	0	1	1	0
1	1	0	0	0	0	1	1	0	1
1	1	1	0	1	1	0	1	1	0

(d) Draw the state diagram. **[5 points]**



(e) This circuit is actually a pattern detector. Assuming that the circuit is starting from "00 (AB)" state, what bit pattern does this circuit detect? [2 points]

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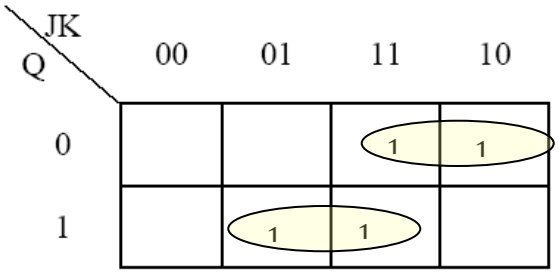
4. Convert a T flip-flop to a JK flip-flop by including input gates to the T flip flop. The gates needed for the input of the T flip flop can be determined by means of sequential circuit design procedures. The sequential circuit to be considered will have one T flip flop and two inputs, J and K.

(a) Tabulate the state table. **[10 points]**

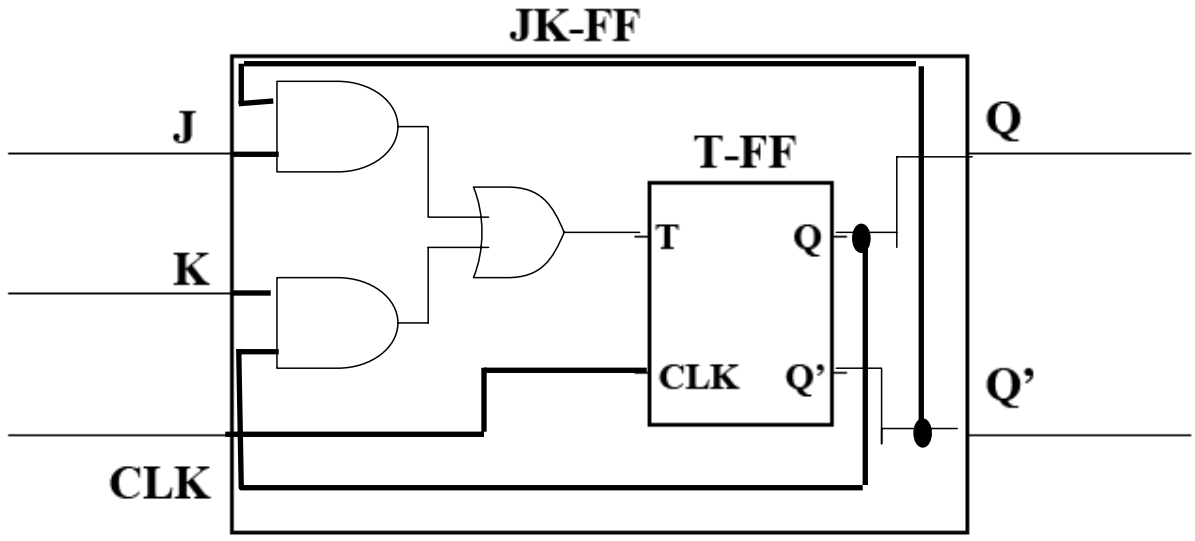
Present State	Inputs		Next State	Flip Flop Input
Q	**J**	**K**	**Q**	**T**
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

(b) **Simplify the equation for T using the K-Map method. [5 points]**



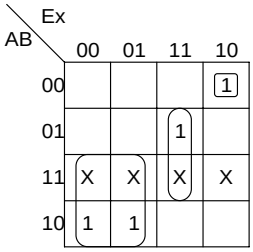
T=Q'J+QK

(c) Put your answer in the form of a logic diagram below. [5 points]

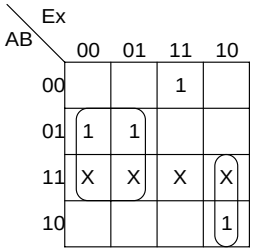


5. Design a sequential circuit with two D flip flops, and two inputs, E and x. If E =0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 10 to 01 back to 00, and repeats. The circuit is to be designed by treating the unused state(s) as don't care condition(s). The final circuit must be analyzed to ensure that it is **self-correcting. [25 points]**

Present State		**Inputs**		**Next State**		**Flip Flop Inputs**	
A	**B**	**E**	**x**	**A**	**B**	$\mathbf{D_A}$	$\mathbf{D_B}$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0
0	0	1	1	0	1	0	1
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	1	0	1
1	0	1	1	0	0	0	0
1	1	0	0			X	X
1	1	0	1			X	X
1	1	1	0			X	X
1	1	1	1			X	X



D_A=AE' + BEx + A'B'Ex'

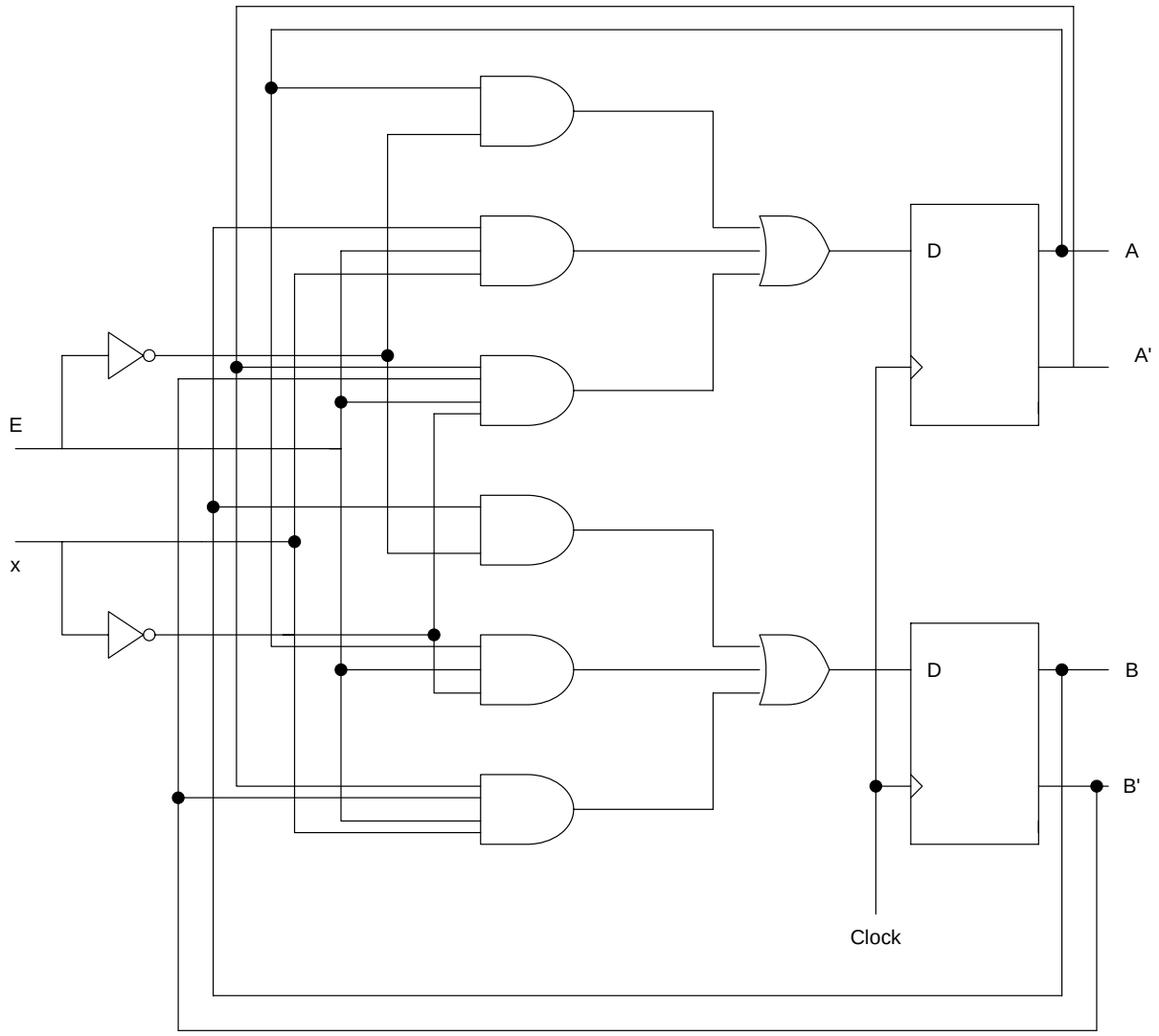


D_B = BE' + AEx' + A'B'Ex

Analysis of unused state:

Present State		**Inputs**		**Next State**		**Flip Flop Inputs**	
A	**B**	**E**	**x**	**A**	**B**	**D_A**	**D_B**
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	0	0	1	0	1
1	1	1	1	0	0	1	0

The circuit is self- correcting!


D
A
A'
E
x
D
B
B'
Clock