Faculty of Engineering

ELECTRICAL AND ELECTRONIC ENGINEERING DEPARTMENT

EENG115/INFE115 Introduction to Logic Design

EENG211/INFE211 Digital Logic Design I

Fall 2011-12

Instructors:

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Final EXAMINATION

Jan. 10, 2012

Duration : 120 minutes

Number of Problems: 5

Good Luck

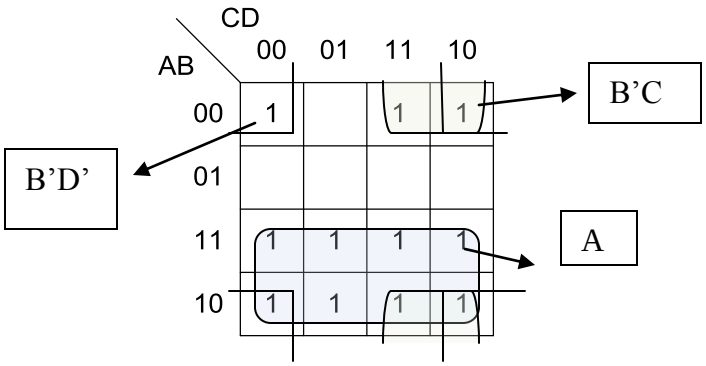
STUDENT'S	
NUMBER	
NAME	**SOLUTIONS**
SURNAME	
GROUP NO	

Problem	Achieved	Maximum
1		20
2		20
3		20
4		20
5		20
TOTAL		100

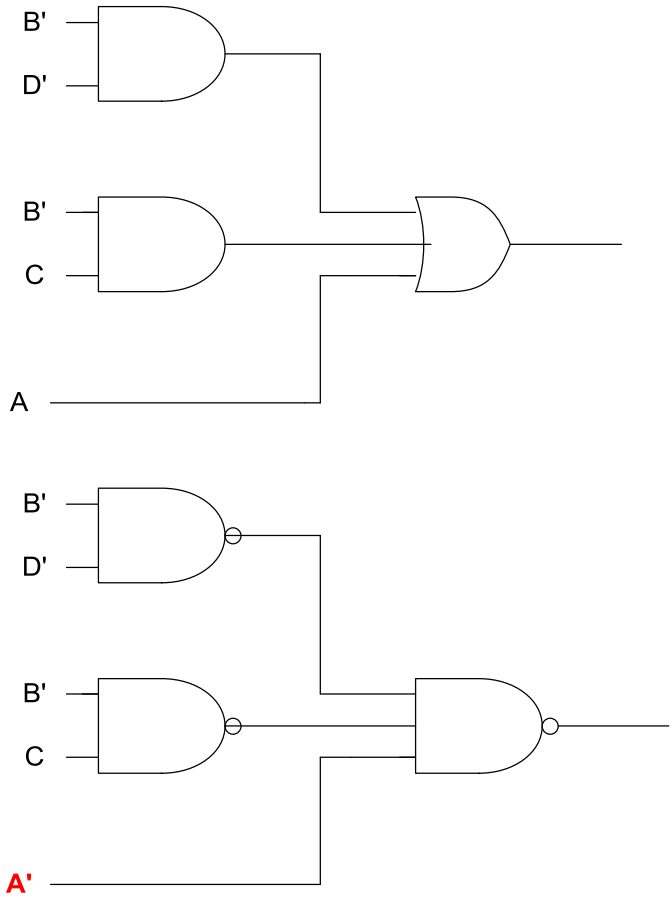
Question 1 (20 points)

a) Simplify the following function and implement it by using two-level NAND gates. (**10 pts**)

$$F(A,B,C,D) = A'B'C + AC' + ACD + ACD' + A'B'D'$$

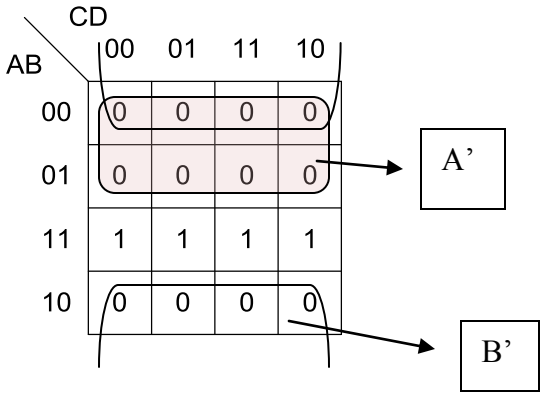


F(A,B,C,D) = A + B'C + B'D'

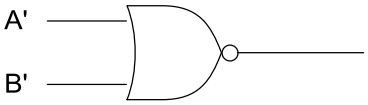


b) Simplify the following function and implement it by using two-level NOR gates. (**10 pts**)

$$F(A,B,C,D) = (A \oplus B)'(AC' + BC) = (A'B' + AB)(AC' + BC) = ABC' + ABC$$



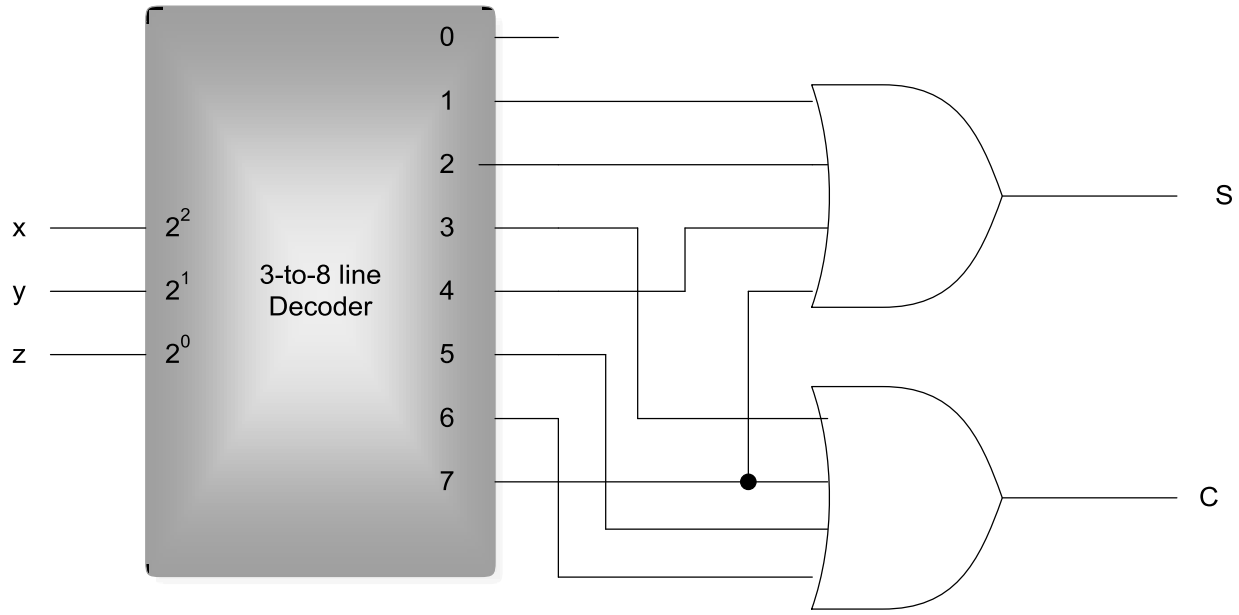
F'(A,B,C,D)=A' +B'
F(A,B,C,D)=(A' + B')'



Question 2 (20points):
Implement a full adder circuit by using:

a) 3 – to - 8 line Decoder (**10 pts**)
b) 4 X 1 Multiplexers. (**10 pts**)

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



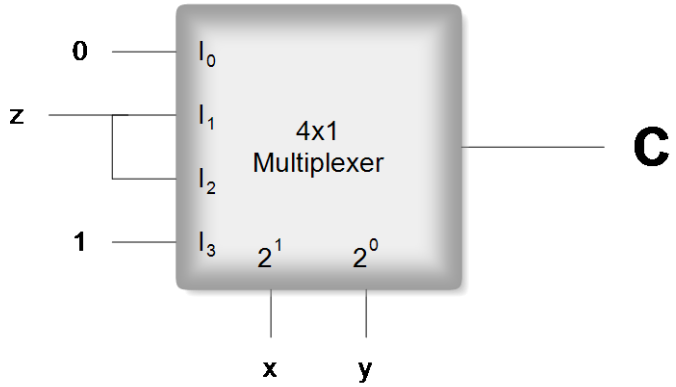
x	y	z	C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

I_0=0

I_1=z

I_2=z

I_3=1



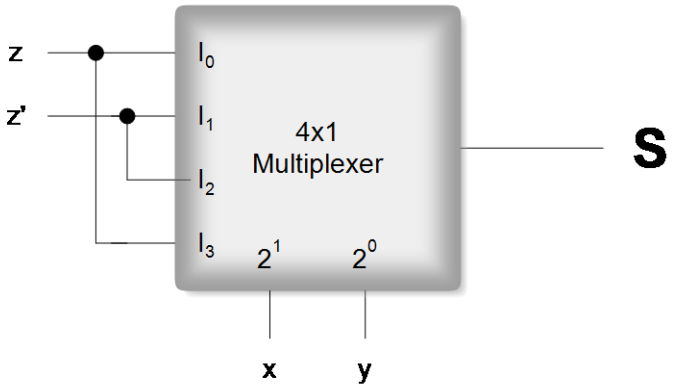
x	y	z	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$I_0=z$

$I_1=z'$

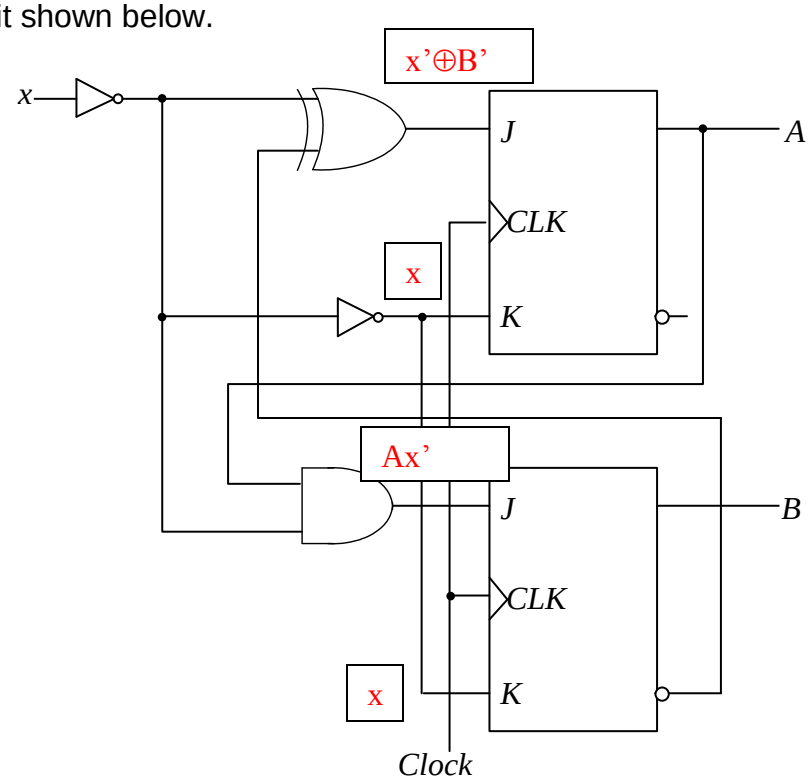
$I_2=z'$

$I_3=z$



Question 3 (20 points):

Analyze the following circuit to derive the state table and the state diagram of the sequential circuit shown below.



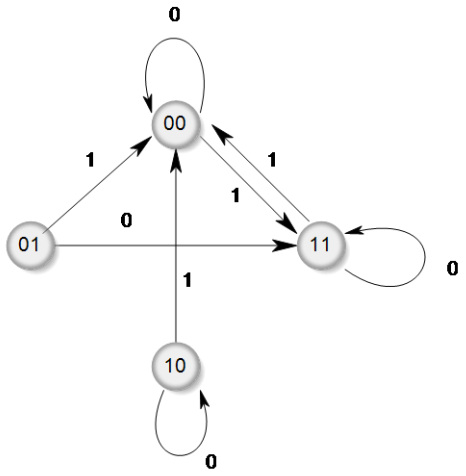
$J_A= x'\oplus B'$

$K_A=x$

$J_B=Ax'$

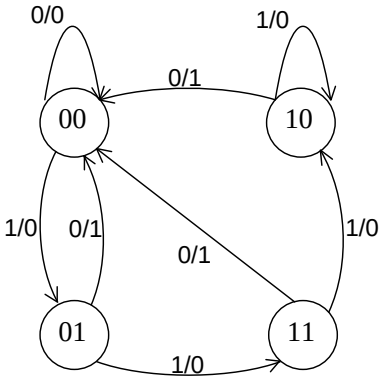
$K_B=x$

Present State		Input	Next State		Flip-flop inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1
0	1	0	1	1	1	0	0	0
0	1	1	0	0	0	1	1	1
1	0	0	1	0	0	0	0	0
1	0	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	1	0	0	0	1	0	1



Question 4 (20 points):

Assume that the following state diagram is provided.



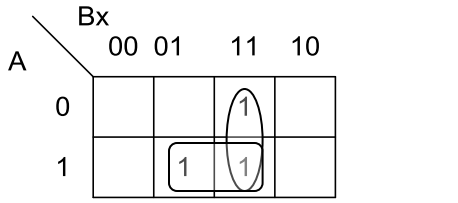
a) Starting from state 00 determine state transitions and output sequence that will be generated when an input sequence of 01011011011110 is applied. (**5 pts)**
b) Design a sequential circuit using D flip fops. (**15 pts**)

a)

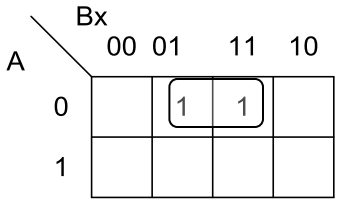
State	00	00	01	00	01	11	00	01	11	00	01	11	10	10	00
Input	0	1	0	1	1	0	1	1	0	1	1	1	1	0	
Output	0	0	1	0	0	1	0	0	1	0	0	0	0	1	

b)

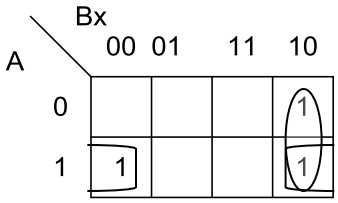
Present State		Input	Next State		Output	Flip-flop Inputs	
A	B	x	A	B	y	D_A	D_B
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	1	0	0
0	1	1	1	1	0	1	1
1	0	0	0	0	1	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	1	0	0	1	0



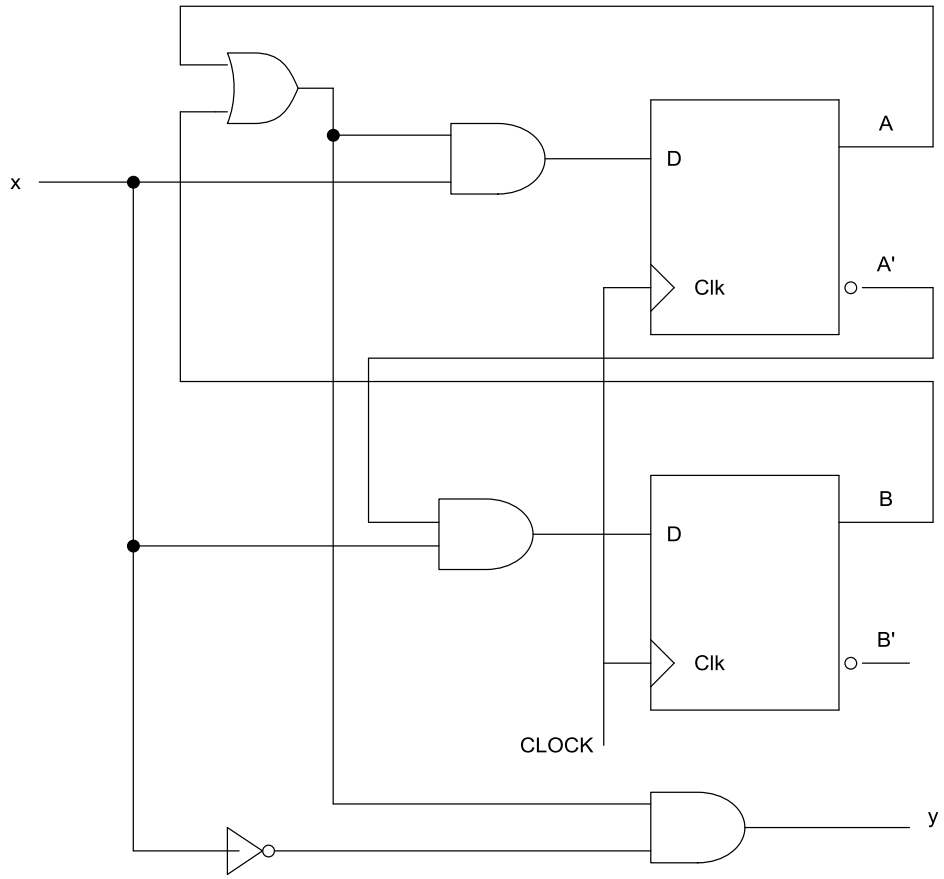
$D_A = Ax + Bx = (A + B)\,x$



$D_B = A'x$



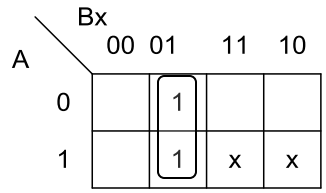
$y = Bx' + Ax' = (A + B)x'$


x
D
A
Clk
A'
D
B
Clk
B'
CLOCK
y

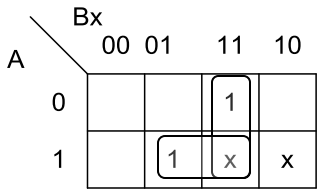
Question 5 (20 points):

Design a counter which counts down, with the repeated sequence: 2, 1, 0, when the input to the counter circuit is 1. The counter doesn't count (stays at the same state) when the input is 0. The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. Use T flip flops in your design.

Present State		Input	Next State		Flip-flop Inputs	
A	**B**	**x**	**A**	**B**	**T_A**	**T_B**
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	1	0	0	0	1
1	0	0	1	0	0	0
1	0	1	0	1	1	1
1	1	0			x	x
1	1	1			x	x



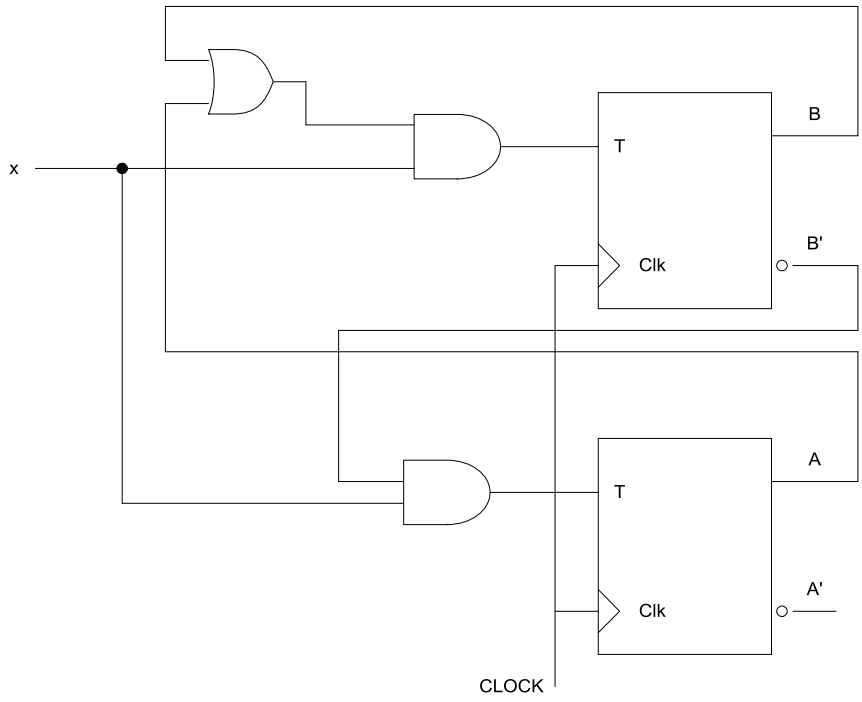
$T_A=B'x$



$T_B=Ax+Bx=(A+B)x$

Analysis for unused state:

Present State		Input	Next State		Flip-flop inputs	
A	B	x	A	B	T_A	T_B
1	1	0	1	1	0	0
1	1	1	1	0	0	1


x
T
Clk
B
B'
T
Clk
A
A'
CLOCK