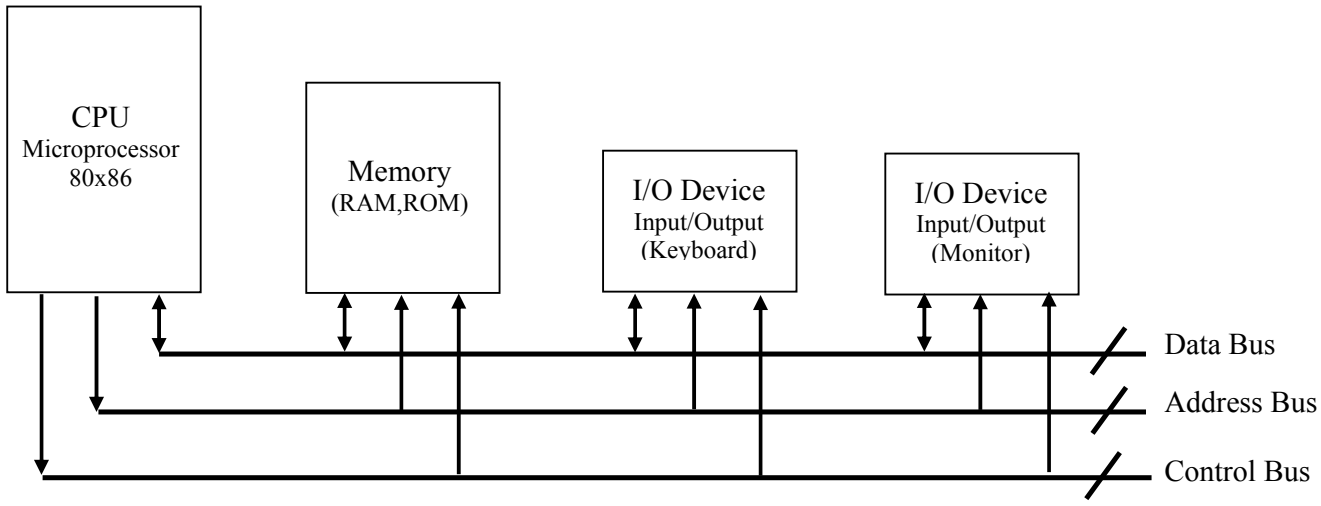
EEE 410 – Microprocessors I

Spring 04/05 – Lecture Notes # 15

Outline of the Lecture

- **Basic Computer Architecture**

BASIC COMPUTER ARCHITECTURE



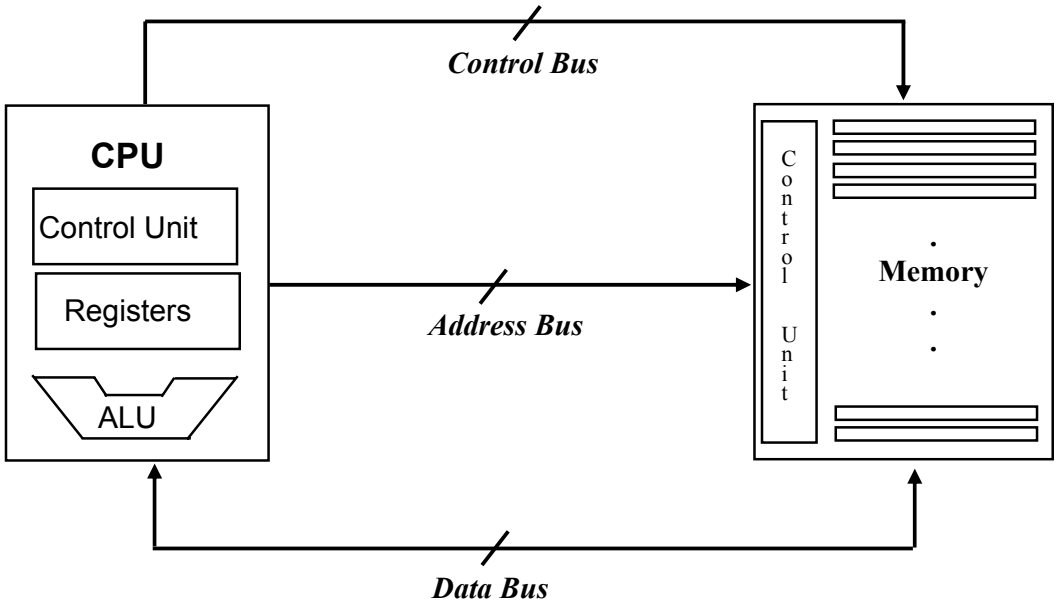
CPU **:** Central Processing Unit/Microprocessor; the *Brain* and the *Heart* of the Computer. Executes (processes) the information stored in memory.

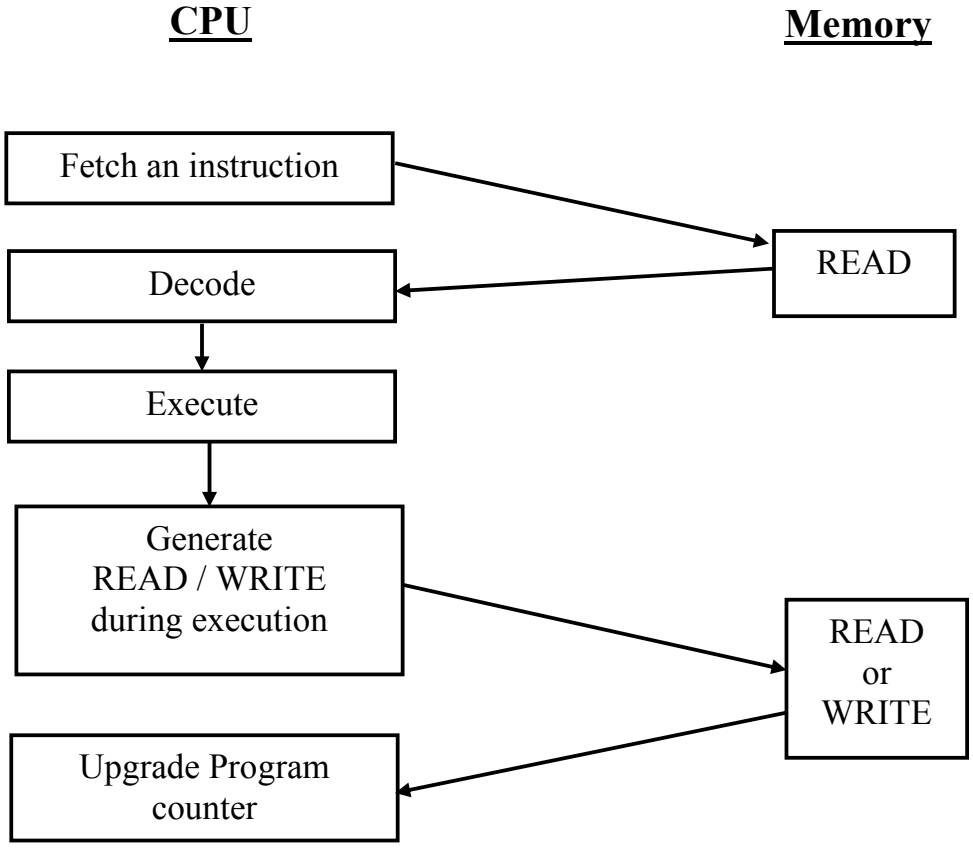
Memory **:** Memory is the primary storage for the programs and data (RAM, ROM)

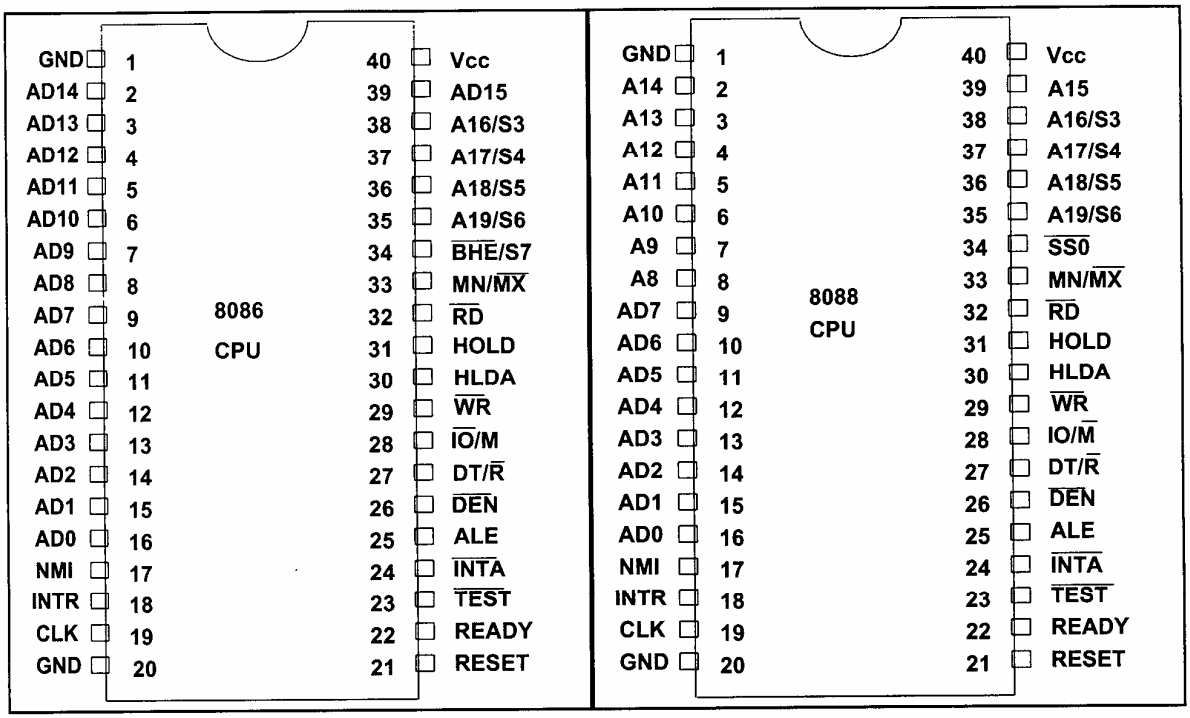
I/O **:**
- Drives the disks (secondary storage units):Hard Disk, Floppy Disks etc.
- Monitor (CRT –*Cathode Ray Tube*)
- Keyboard
- Printer
- Mouse
- Fax, Modem

Buses **:** A bus is defined to be a bundle of wires. There are 3 types of buses
- Address Bus (Unidirectional)
- Data Bus (Bidirectional)
- Control Bus (Unidirectional)

- **Time Sequencing during an instruction execution**







(a) 8086 Microprocessor (b) 8088 Microprocessor

Pin descriptions of 8086 Microprocessor

Data Bus: - In 8086 microprocessor Pins AD0 – AD15 are used for the data bus.
- However the same pins are also used for Address bus as well.
- The ALE (Address Latch Enable –pin 25) signals whether the information on pins AD0 – AD15 is used address or data.
- When the data is sent out or in, the case when ALE is low indicates that AD0-AD15 will be used as data bus.
- When the address data is sent out, the ALE is high indicating that AD0-AD15 will be used as address bus
- This process of separating address and data from pins AD0-AD15 is called demultiplexing.

Address Bus: - The 8086 CPU is has 20-bit address bus, where the AD0-AD15 and A16-A20 are used as the address bus. To demultiplex the address signals from the address/data pins (AD0-AD15) a latch must be used to grab the addresses.
- In 8086 microprocessor the address bus is 20-bit wide, however only 16-bit is shared with data bus (AD0-AD15) through demultiplexing.
- The most widely used latch for demultiplexing is 74LS373 IC (see Figure 9-3 below: Note that for 8088 the address bus is 20 bit and data bus is 8-bit. So only 8-bit is latched).

Control Bus : is used to indicate
- When a valid address is on the address bus
- In which direction data are to be transferred over the data bus (in/out)
- When external devices can read/write data on the data bus.
- When valid read/write data are on the data bus.
- Etc.

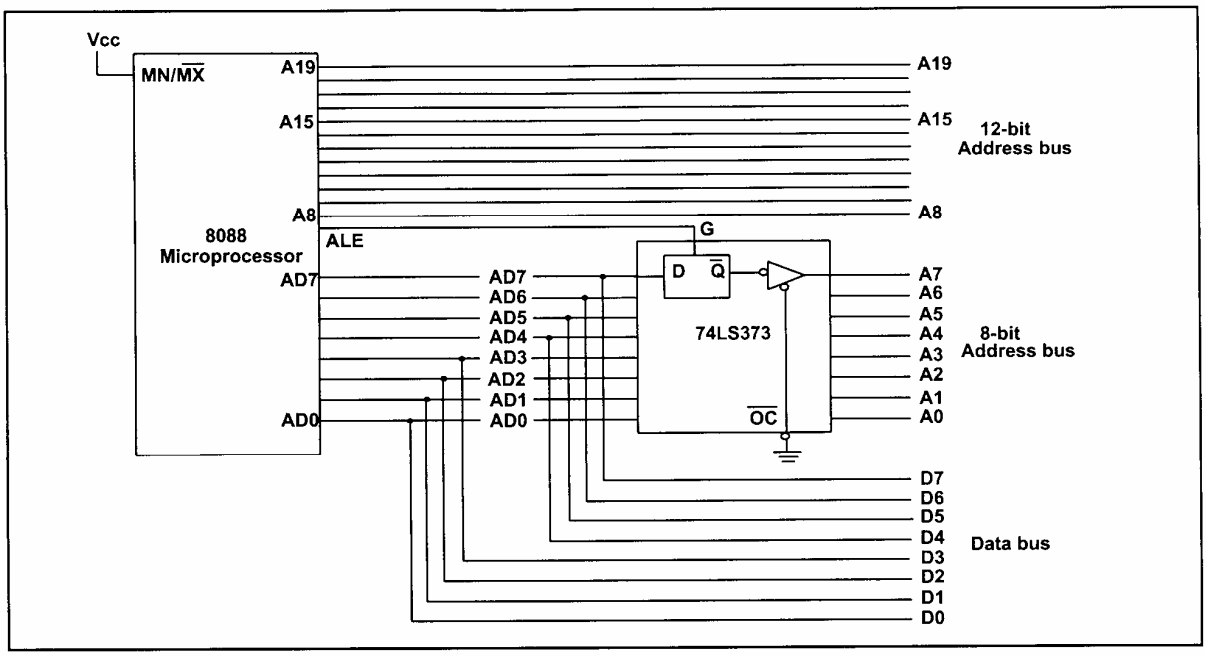


Figure 9-3. Role of ALE in Address/Data Demultiplexing

Pin Descriptions of the Control Signals of 8086 CPU

Pin	Name	Function
34	$\overline{\textbf{BHE}}$ (Bus High Enable)	It provides control signal to distinguish between the low byte and the high byte of the 16-bit data. (Active-low)
17	**NMI** (Nonmaskable Interrupt)	This signal will make the microprocessor to jump to the interrupt vector table after it finishes the current instruction. This interrupt cannot be masked by software.
18	**INTR** (Interrupt Request)	If it is activated, it will finish the execution of the current instruction and respond with the interrupt acknowledge operation. In IBM PC it is connected to the interrupt controller.
19	**CLK** (Clock)	It acts as the heartbeat of the CPU. Intel has designed the 8284 clock generator and a driver to be used for the processor.
21	**RESET**	To terminate the present activities of the microprocessor, a high signal is applied for the RESET pin.
22	**READY**	It is an input signal used to insert a wait state for slower memories and I/O. It inserts wait states when it is low.
23	$\overline{\textbf{TEST}}$	This is input from the 8087 coprocessor. During execution of a wait instruction, the CPU checks this signal. If it is low, execution of the signal will continue; if not, it will stop executing.
24	$\overline{\textbf{INTA}}$ (Interrupt acknowledge)	Active-low output signal. Informs interrupt controller that INTR has occurred and that the vector number is available on the lower 8 lines of the data bus
25	**ALE** (Address Latch Enable)	Active-high output signal. Indicates that a valid address is available on the external address bus. See Figure 9-3.
26	$\overline{\textbf{DEN}}$ (Data Enable)	Active-low output signal. This allows the isolation of the CPU from the system bus.
27	**DT/$\overline{\textbf{R}}$** (Data transmit/receive)	Active-low output signal used to control the direction of the data flow (transmit/receive)

28	**$\overline{\text{IO}}$/M** (memory or input/output)	Indicates whether the address bus is accessing memory or I/O device. In 8086, when it is high, it is accessing the memory and when it is low , it is accessing the I/O.
29	**$\overline{\text{WR}}$** (Write)	Active-low output signal. Indicates that the data on the data bus is being written to memory or I/O. Used along with pin 28 for write operations.
30	**HLDA** (hold acknowledge)	Active-high output signal. After input on HOLD, the CPU responds with HLDA to signal that ***DMA (Direct Memory Access)*** controller can use the bus.
31	**HOLD** (hold)	Active-high input from the DMA controller which indicates that the device is requesting access to memory and I/O space and that the CPU should release the control of the local bus.
32	**$\overline{\text{RD}}$** (Read)	Active-low output signal. Indicates that the data on the data bus is being read from the memory or I/O. Used along with pin 28 for read operations.

Basic Busses for a computer:

Every computer must have three basic busses in order to communicate: Address bus, data bus, and the control bus. The figure below shows the basic busses of 8088 based-computer. Note that the 3 control signals from 8088: $\overline{\text{WR}}$, $\overline{\text{RD}}$, and IO/$\overline{\text{M}}$ are used to generate 4 new control signals ($\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$) by using a decoder circuit.

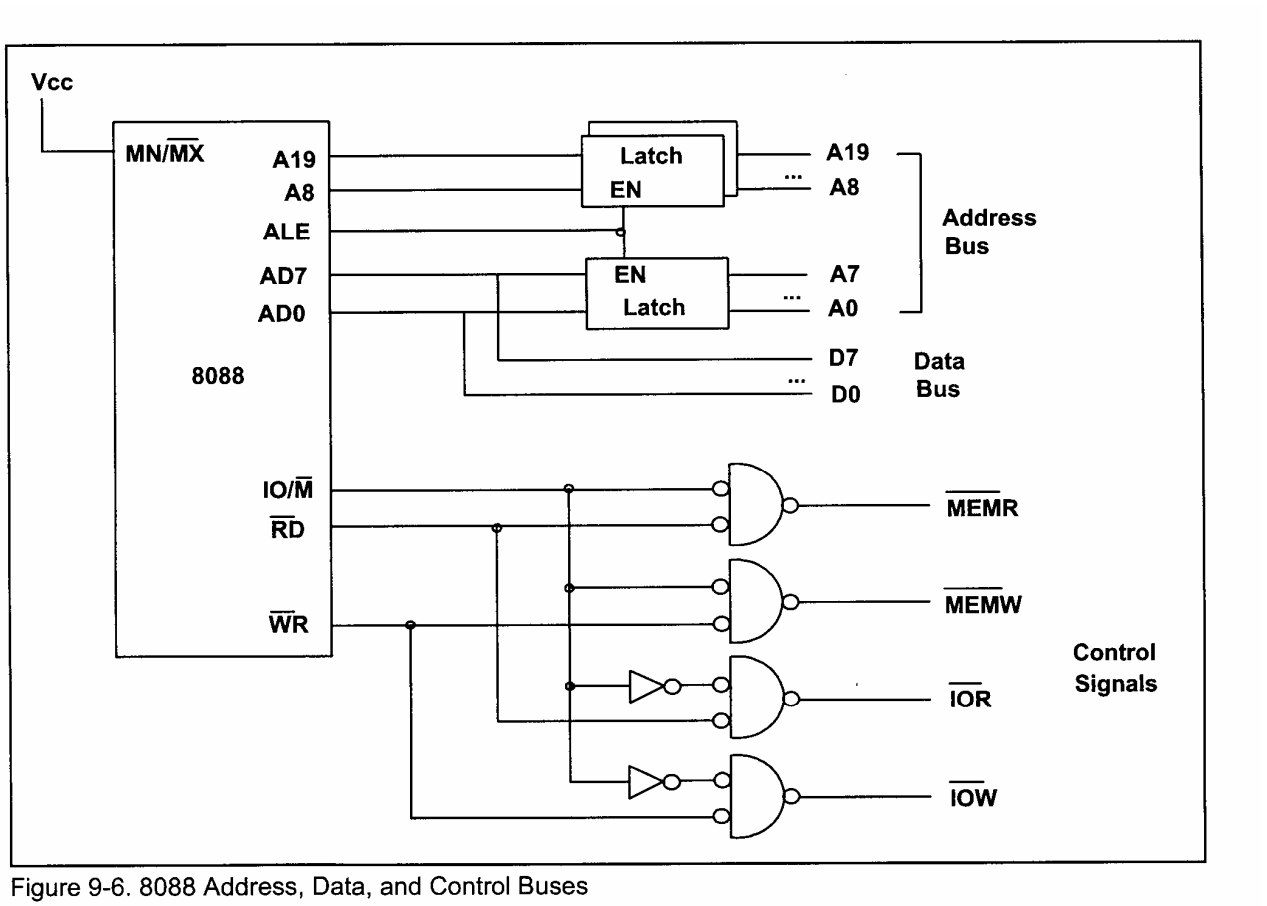


Figure 9-6. 8088 Address, Data, and Control Buses

Direct Memory Access (DMA)

In computers there is often need to transfer a large amount of data between the memory and peripherals such as hard disk. In such a case using the CPU to transfer data is too slow, since the data first must be fetched into the CPU and then sent to its destination.

For this reason Direct Memory Access controller is used to bypass the CPU and provide a direct connection between the peripherals and memory, thus transferring the data as fast as possible.