Experiment 1

Basic Logic Gates

#	Student No.	Name Surname	Signature
1			
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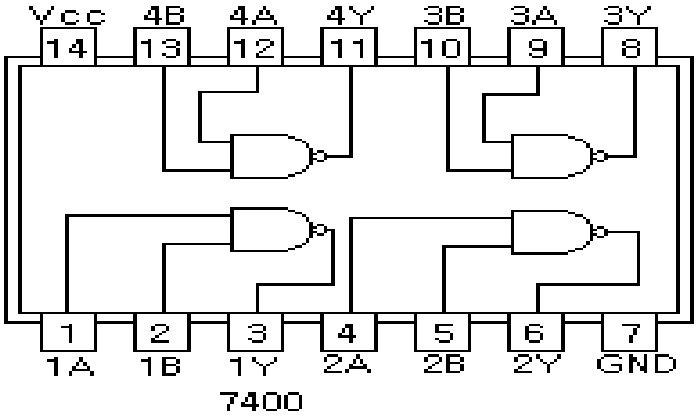
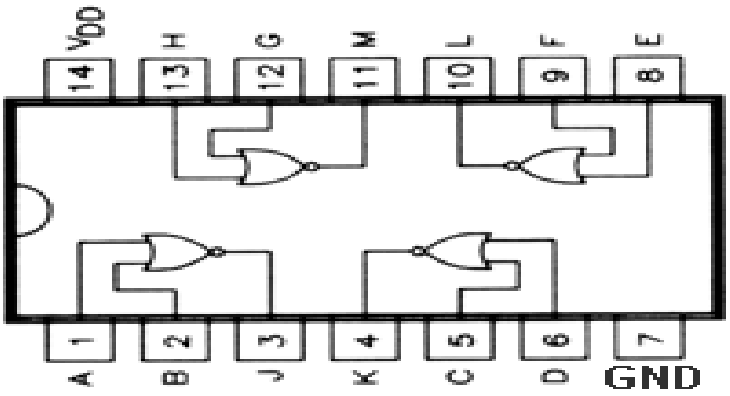
Objectives:

To demonstrate the operation and characteristics of a TTL logic gate (7400) and a CMOS logic gate (4001) and to show how each of them can be used to perform any of the three basic logic functions.



7400

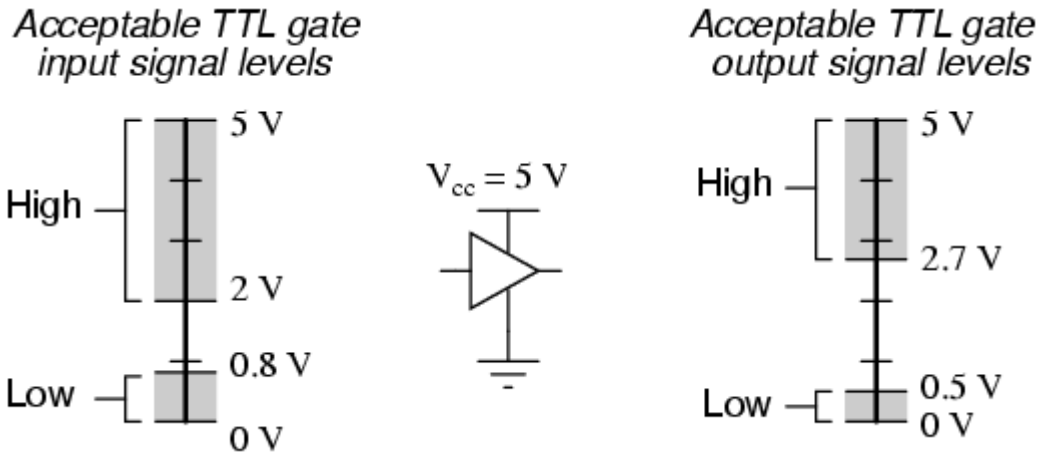


4001 NOR Gate

Logic Gates:

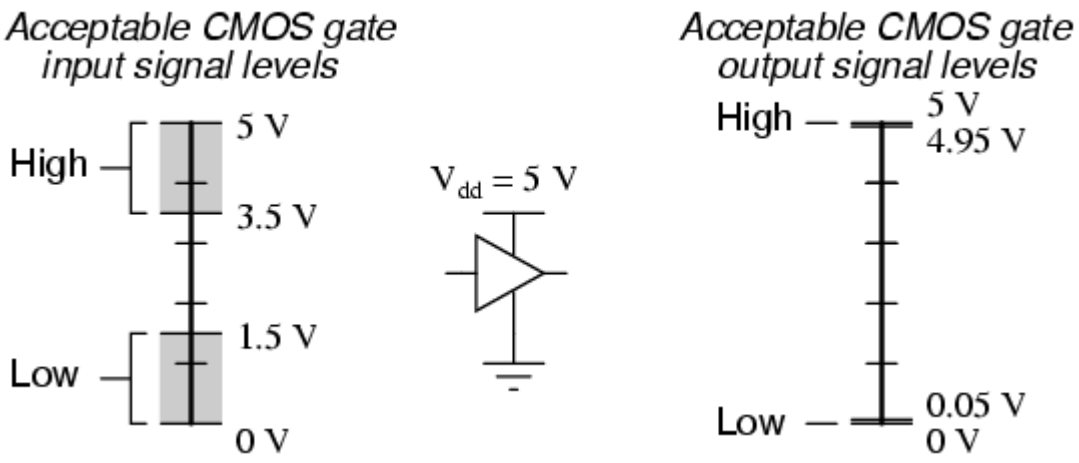
Logic gates are electronic circuits that operate on one or more input signals to produce an output signal. Electrical signals such as voltages or currents exist as analog signals having values over a given continuous range, say, 0 to 3 V, but in a digital system these voltages are interpreted to be either of two recognizable values, 0 or 1.

Voltage-operated logic circuits respond to two separate voltage levels that represent a binary variable equal to logic 1 or logic 0. For example, a particular digital system may define logic 0 as a signal equal to 0 V and logic 1 as a signal equal to 3 V. In practice, each voltage level has an acceptable range. The input terminals of digital circuits accept binary signals within the allowable range and respond at the output terminals with binary signals that fall within the specified range.



If a voltage signal ranging between 0.8 volts and 2 volts were to be sent into the input of a TTL gate, there would be no certain response from the gate. Such a signal would be considered uncertain, and no logic gate manufacturer would guarantee how their gate circuit would interpret such a signal. As you can see, the tolerable ranges for output signal levels are narrower than for input signal levels, to ensure that any TTL gate outputting a digital signal into the input of another TTL gate will transmit voltages acceptable to the receiving gate. The difference between the tolerable output and input ranges is called the noise margin of the gate. For TTL gates, the low-level noise margin is the difference between 0.8 volts and 0.5 volts (0.3 volts), while the high-level noise margin is the difference between 2.7 volts and 2 volts (0.7 volts). Simply put, the noise margin is the peak amount of spurious or "noise" voltage that may be superimposed on a weak gate output voltage signal before the receiving gate might interpret it wrongly.

CMOS gate circuits have input and output signal specifications that are quite different from TTL. For a CMOS gate operating at a power supply voltage of 5 volts, the acceptable input signal voltages range from 0 volts to 1.5 volts for a "low" logic state, and 3.5 volts to 5 volts for a "high" logic state. "Acceptable" output signal voltages (voltage levels guaranteed by the gate manufacturer over a specified range of load conditions) range from 0 volts to 0.05 volts for a "low" logic state, and 4.95 volts to 5 volts for a "high" logic state:



Integrated Circuits:

An integrated circuit (IC) is fabricated on a die of a silicon semiconductor crystal, called a chip, containing the electronic components for constructing digital gates. The complex chemical and physical processes used to form a semiconductor circuit are not a subject of this experiment.

The various gates are interconnected inside the chip to form the required circuit. The chip is mounted in a ceramic or plastic container, and connections are welded to external pins to form the integrated circuit. The number of pins may range from 14 on a small IC package to several thousand on a larger package. Each IC has a numeric designation printed on the surface of the package for identification.

Vendors provide data sheets, data books, catalogs, and Internet websites that contain descriptions and information about the ICs that they manufacture.

Levels of Integration:

Digital ICs are often categorized according to the complexity of their circuits, as measured by the number of logic gates in a single package. The differentiation between those chips which have a few internal gates and those having hundreds of thousands of gates is made by customary reference to a package as being either a small-, medium-, large-, or very large-scale integration device.

Small - scale integration (SSI) devices contain several independent gates in a single package. The inputs and outputs of the gates are connected directly to the pins in the package. The number of gates is usually fewer than 10 and is limited by the number of pins available in the IC.

Medium - scale integration (MSI) devices have a complexity of approximately 10 to 1,000 gates in a single package. They usually perform specific elementary digital operations. MSI digital functions are introduced in Chapter 4, of the course textbook, as decoders, adders, multiplexers and in Chapter 6 too as registers and counters.

Large - scale integration (LSI) devices contain thousands of gates in a single package. They include digital systems such as processors, memory chips, and programmable logic devices. Some LSI components are presented in Chapter 7, course textbook .

Very large - scale integration (VLSI) devices now contain millions of gates within a single package. Examples are large memory arrays and complex microcomputer chips. Because of their small size and low cost, VLSI devices have revolutionized the computer system design technology, giving the designer the capability to create structures that were previously uneconomical to build.

Digital Logic Families:

Digital integrated circuits are classified not only by their complexity or logical operation, but also by the specific circuit technology to which they belong. The circuit technology is referred to as a digital logic family. Each logic family has its own basic electronic circuit upon which more complex digital circuits and components are developed. The basic circuit in each technology is a NAND, NOR, or inverter gate.

The electronic components employed in the construction of the basic circuit are usually used to name the technology. Many different logic families of digital integrated circuits have been introduced commercially. The following are the most popular:

TTL transistor–transistor logic;
ECL emitter-coupled logic;
MOS metal-oxide semiconductor;
CMOS complementary metal-oxide semiconductor.

TTL is a logic family that has been in use for 50 years and is considered to be standard. ECL has an advantage in systems requiring high-speed operation. MOS is suitable for circuits that need high component density, and CMOS is preferable in systems requiring low power consumption, such as digital cameras, personal media players, and other handheld portable devices. Low power consumption is essential for VLSI design; therefore, CMOS has become the dominant logic family, while TTL and ECL continue to decline in use. The most important parameters distinguishing logic families are listed below:

Fan - out specifies the number of standard loads that the output of a typical gate can drive without impairing its normal operation. A standard load is usually defined as the amount of current needed by an input of another similar gate in the same family.

Fan - in is the number of inputs available in a gate.

Power dissipation is the power consumed by the gate that must be available from the power supply.

Propagation delay is the average transition delay time for a signal to propagate from input to output. For example, if the input of an inverter switches from 0 to 1, the output will switch from 1 to 0, but after a time determined by the propagation delay of the device. The operating speed is inversely proportional to the propagation delay.

Noise margin is the maximum external noise voltage added to an input signal that does not cause an undesirable change in the circuit output.

Active-High and Active-Low:

When working with ICs and microcontrollers, you'll likely encounter pins that are active-low and pins that are active-high. Simply put, this just describes how the pin is activated. If it's an active-low pin, you must "pull" that pin LOW by connecting it to ground. For an active high pin, you connect it to your HIGH voltage (usually 3.3V/5V).

Electrostatic Discharge (ESD) and IC Handling:

Electrostatic discharge (ESD) is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown.

Body capacitance is the physical property of the human body that has it act as a capacitor. Like any other electrically-conductive object, a human body can store electric charge if insulated. The actual amount of capacitance varies with the surroundings. Tyipically around 100-200 pF with respect to ground. Synthetic fabrics and friction can charge a human body to about 3 kV.

Low potentials may not have any notable effect, but some electronic devices can be damaged by modest voltages of 100 volts. Electronics factories are very careful to prevent people from becoming charged up. A whole branch of the electronics industry deals with preventing static charge build-up and protecting products against electrostatic discharge.

Thus we must hold the IC from the ceramic/plastic container and not from the pins.

A. NAND GATES

An introductory note: Logic operations are performed in logical gates, which receive inputs and generate outputs accordingly. In this lab, we will use logical gates encapsulated inside integrated circuits (ICs). An IC contains a certain number of logical gates that can be used when we connect the IC power lines. Moreover, the logical status is displayed on LEDs which emit light according to that value. Herein, Green represents logic 0 and Red represents logic 1.

A1. Connect one of the four gates in the 7400 IC as shown in Fig. 1.1 and record your data in Table 1A. The inputs will come from the data switches **SW_0** and you will monitor the output states with LED display **L_1**. (Binary 1 = Red, Binary 0 = Green)

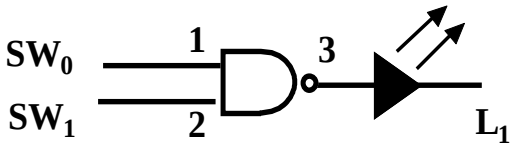
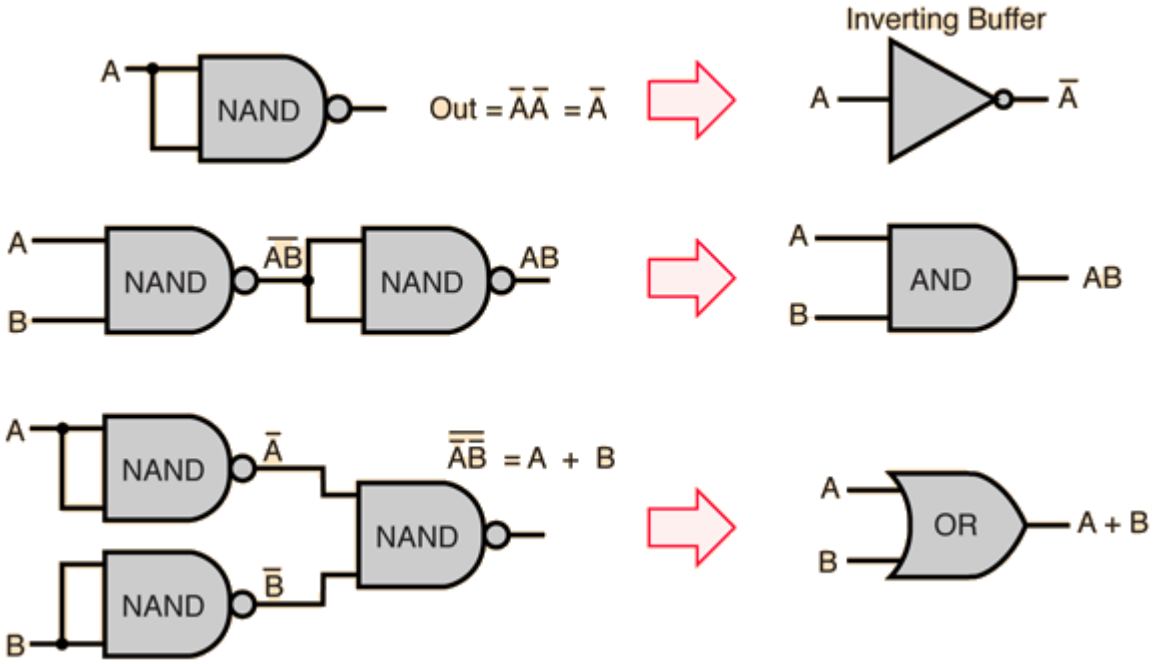


Fig 1.1

Table 1A

SW_1	SW_0	OUTPUT (L_1)
0	0	
0	1	
1	0	
1	1	



A2. Connect one of the four gates in the 7400 IC as shown in Fig. 1.2 and record your data in table 2A. The input will come from data switch $\mathbf{SW_0}$. You will monitor the input and output states with $\mathbf{L_0}$ and $\mathbf{L_1}$ LED displays.

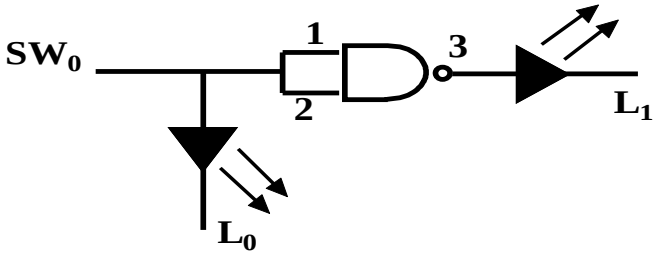


Fig. 1.2

Table 2A

INPUT $(SW_0)=(L_0)$	OUTPUT (L_1)
0 (Green)	
1 (Red)	

A3. Wire the circuit shown in Fig. 1.3. With $\mathbf{SW_0}$ and $\mathbf{SW_1}$, apply the states shown in table 3A. Record the output state for each set of input states by observing the LED display $\mathbf{L_1}$.

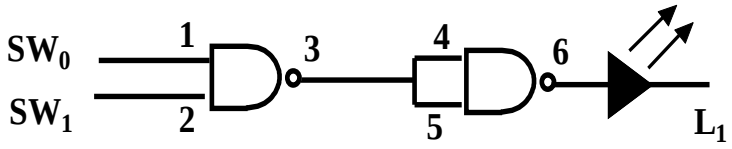


Fig 1.3

Table 3A

SW_1	SW_0	OUTPUT (L_1)
0	0	
0	1	
1	0	
1	1	

B. NOR GATES

B1. Connect one of the four gates in the 4001 IC as shown in Fig. 1.4 and record your data in Table 1B. The inputs will come from the data switches $\mathbf{SW_0}$ and $\mathbf{SW_1}$. You will monitor the output states with LED $\mathbf{L_0}$. . (Binary 1 = Red, Binary 0 = Green)

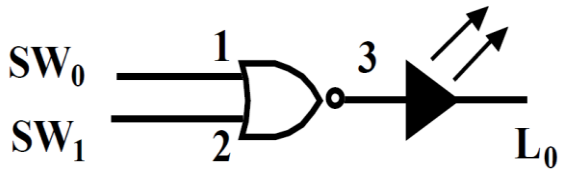


Fig 1.4

Table 1B

$\mathbf{SW_1}$	$\mathbf{SW_0}$	**OUTPUT (L0)**
0	0	
0	1	
1	0	
1	1	

B2. Connect one of the four gates in the 4001 IC as shown in Fig. 1.5 and record your data in table 2B. The **input** will come from data switch $\mathbf{SW_0}$. You will monitor the **input** and **output** states with $\mathbf{L_0}$ and $\mathbf{L_1}$ LED displays, respectively.

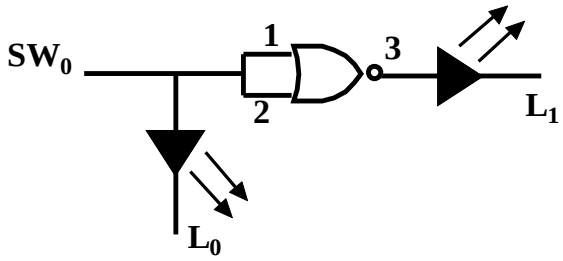


Fig 1.5

Table 2B

INPUT **(SW_0)**	OUTPUT **(L1)**
0	
1	

B3. Wire the circuit shown in Fig. 1.6 with $\mathbf{SW_0}$ and $\mathbf{SW_1}$ as inputs. Apply the states shown in table 3B, observing the corresponding output generated at $\mathbf{L_0}$. Tabulate the data in Table 3B.

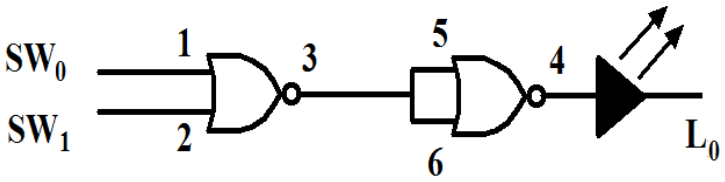


Fig 1.6

Table 3A

$\mathbf{SW_1}$	$\mathbf{SW_0}$	**OUTPUT (L1)**
0	0	
0	1	
1	0	
1	1	

Questions:

1. Fill the following truth tables.

A	B	A AND B	A NAND B	A OR B	A NOR B	A XOR B	A XNOR B
A	B	A.B	$\overline{A.B}$	A+B	$\overline{A+B}$	A⊕B	$\overline{A \oplus B}$
0	0						
0	1						
1	0						
1	1						

A	NOT A
A	$\overline{A}$
0	
1	

2. Implement an OR gate using the 7400 NAND Gate IC.

3. Implement an AND gate using the 4001 NOR gate IC.

4. What do Vcc and Vdd Stand for?

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How do we recognize pin #1 in an IC?

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5. What is a logic gate?

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What is an IC?

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6. How TTL and CMOS gates differ in the acceptable input and output signal levels?

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7. What do we mean by Active-High and Active-Low design?

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8. How should we handle ICs and why?

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9. Name the most popular logic families and define the most important parameters distinguishing logic families.

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